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BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Masahiro ARAI
CLOCK SIGNAL TRANSMITTING SYSTEM, DIGITAL SIGNAL TRANSMITTING SYSTEM, CLOCK SIGNAL TRANSMITTING METHOD, AND DIGITAL SIGNAL TRANSMITTING METHOD
Our Ref. Q61788

Dear Sir:

Attached hereto is the application identified above including 46 sheets of the specification, claims, 24 sheets of formal drawings, executed Assignment and PTO 1595 form, and executed Declaration and Power of Attorney. Also enclosed is the Information Disclosure Statement with form PTO-1449 and references.

The Government filing fee is calculated as follows:

Total claims	38	-	20	=	18	x	$18.00	=	$324.00
Independent claims	2	-	3	=		x	$80.00	=	$.00
Base Fee									$710.00
TOTAL FILING FEE									**$1034.00**
Recordation of Assignment									$40.00
TOTAL FEE									**$1074.00**

Checks for the statutory filing fee of $1034.00 and Assignment recordation fee of $40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from November 17, 1999 based on Japanese Application No. 327198/1999. The priority document is enclosed herewith.

Respectfully submitted,
SUGHRUE, MION, ZINN,
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Clock Signal Transmitting System, Digital Signal Transmitting System, Clock Signal Transmitting Method, and Digital Signal Transmitting Method

Background of the Invention

Field of the Invention:

The present invention relates to a system and method for generating a transmission digital signal from a source digital signal and reproducing the source digital signal as a reproduced digital signal from the transmission digital signal, and in particular, to a system and method for suppressing an electromagnetic noise generated by the transmission digital signal. The source digital signal is, for example, a clock signal and a data signal.

Prior Art:

Since a clock signal is composed of repetitive pulses having the same frequencies, the clock signal has a large spectrum at the clock frequency and its higher harmonic frequencies. When the clock signal is transmitted through a transmission path, the signal radiates electromagnetic noise having these frequencies. A data signal does not have a higher periodicity than the clock signal. However, a video signal and an audio signal which have been band-compressed have a high entropy. Thus, these signals have a high periodicity and large spectrums at 1/2 frequency of the clock signal and its higher harmonic frequencies. Therefore, a data signal transmitted through a transmission path radiates electromagnetic noise at these

frequencies.

Conventionally, in order to suppress the electromagnetic noise, the voltage amplitudes or current amplitudes of a clock signal and a data signal are decreased. In addition, a differential transmission system such as ECL (Emitter-Coupled Logic) is used.

As a prior art reference, a method and apparatus for suppressing the electromagnetic noise are disclosed in JPA 9-289527. According to the prior art reference, a clock signal is frequency-modulated. The frequency of a spectrum generated from the clock signal is dispersed so as to suppress the electromagnetic noise.

In the method and apparatus of the prior art reference disclosed as JPA 9-289527, a source clock signal is frequency-modulated with a particular frequency so that the frequency of the transmission clock signal is dynamically varied. On the reception side, a PLL removes a modulation signal component so that the source clock signal is reproduced. The frequency change ratio of the transmission clock signal which has been frequency-modulated is supposed to be ± several percent.

Generally, the lock range and capture range of a PLL are as high as several hundred ppm at the maximum. Thus, in the method and apparatus of the prior art reference, the conventional PLL circuit cannot be used to perform adjustment in a several percent range. Instead, a more complicated circuit is required.

Summary of the Invention

In order to overcome the disadvantage mentioned above, the present invention has been made and accordingly, has an object to provide a digital signal transmitting system and method which suppress an electromagnetic noise radiated from a transmission digital signal transmitted through a transmission path with a simpler circuit.

According to a first aspect of the present invention, there is provided a clock signal transmitting system, comprising: a controlling circuit for generating a first control signal and a second control signal which contains synchronization information of the first control signal; a first reference voltage generating circuit for generating a first reference voltage which periodically varies corresponding to the first control signal; a second reference voltage generating circuit for generating a second reference voltage which periodically varies corresponding to the second control signal; a first comparator for comparing a source clock signal with the first reference voltage in order to generate a transmission clock signal; and a second comparator for comparing the transmission clock signal with the second reference voltage in order to generate a reproduced clock signal.

The sum of the first reference voltage generated by the first reference voltage generating circuit and the second reference voltage generated by the second reference voltage generating circuit may be a constant voltage.

The first reference voltage generated by the first reference voltage

generating circuit and the second reference voltage generated by the second reference voltage generating circuit may periodically vary in the same period.

The first reference voltage generating circuit may switch the first reference voltage at a frequency twice as high as the source clock signal, and the second reference voltage generating circuit may switch the second reference voltage at the frequency twice as high as the source clock signal.

The controlling circuit may be disposed on a transmission side.

The controlling circuit may generate the first control signal and the second control signal on the basis of the source clock signal.

The controlling circuit may generate the first control signal and the second control signal on the basis of the transmission clock signal.

The controlling circuit may generate the first control signal and the second control signal on the basis of the source clock signal and the transmission clock signal.

The controlling circuit may generate the second control signal having a frequency which is lower than a frequency of the source clock signal.

The first reference voltage generating circuit may generate the first reference voltage on the basis of the first control signal and the source clock signal.

The first reference voltage generating circuit may generate the first reference voltage on the basis of the first control signal and the

transmission clock signal.

The second reference voltage generating circuit may generate the second reference voltage on the basis of the second control signal and the transmission clock signal.

The second reference voltage generating circuit may generate the second reference voltage on the basis of the second control signal and the reproduced clock signal.

The clock signal transmitting system may further comprise: a local oscillator disposed on a reception side for generating a local clock signal, wherein the second reference voltage generating circuit generates the second reference voltage on the basis of the second control signal and the local clock signal.

The clock signal transmitting system may further comprise: a PLL circuit which inputs the reproduced clock signal as a reference signal in order to output a refined reproduced clock signal.

The clock signal transmitting system may further comprise: a PLL circuit which inputs the reproduced clock signal as a reference signal in order to output a refined reproduced signal, wherein the second reference voltage generating circuit generates the second reference voltage on the basis of the second control signal and the refined reproduced signal.

The clock signal transmitting system may further comprise: a phase compensating circuit for compensating the phase of the reproduced clock

signal.

The first control signal may be the same as the second control signal.

According to a second aspect of the present invention, there is provided a digital signal transmitting system, comprising: the above clock transmitting system; a third comparator for comparing a source data signal with the first reference voltage in order to generate a transmission data signal; and a fourth comparator for comparing the transmission data signal with the second reference voltage in order to generate a reproduced data signal.

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of the best modes of embodiment thereof, as illustrated in the accompanying drawings.

Brief Description of Drawings

Fig. 1 is a block diagram showing the structure of a clock signal transmitting system according to a first embodiment of the present invention;

Fig. 2 is a timing diagram showing the operation of the clock signal transmitting system according to the first embodiment of the present invention;

Fig. 3 is a flow chart showing the operation of a controlling circuit according to the first embodiment of the present invention;

Fig. 4 is a flow chart showing the operation of a first reference voltage generating circuit according to the first embodiment of the present invention;

Fig. 5 is a flow chart showing the operation of a second reference voltage generating circuit according to the first embodiment of the present invention;

Fig. 6 is a flow chart showing the operation of a first comparator according to the first embodiment of the present invention;

Fig. 7 is a flow chart showing the operation of a second comparator according to the first embodiment of the present invention;

Fig. 8 is a block diagram showing the structure of a clock signal transmitting system according to a second embodiment of the present invention;

Fig. 9A is a circuit diagram showing an example of a change detection signal generating circuit of the controlling circuit according to the second embodiment of the present invention;

Fig. 9B is a timing diagram of the change detection signal generating circuit according to the second embodiment of the present invention;

Fig. 10 is a flow chart showing the operation of the controlling circuit according to the second embodiment of the present invention;

Fig. 11 is a block diagram showing the structure of a clock signal transmitting system according to a third embodiment of the present

invention;

Fig. 12 is a block diagram showing the structure of a clock signal transmitting system according to a fourth embodiment of the present invention;

Fig. 13 is a block diagram showing the structure of a clock signal transmitting system according to a fifth embodiment of the present invention;

Fig. 14 is a block diagram showing the structure of a clock signal transmitting system according to a sixth embodiment of the present invention;

Fig. 15 is a block diagram showing the structure of a clock signal transmitting system according to a seventh embodiment of the present invention;

Fig. 16 is a block diagram showing the structure of a clock signal transmitting system according to an eighth embodiment of the present invention;

Fig. 17 is a block diagram showing the structure of a clock signal transmitting system according to a ninth embodiment of the present invention;

Fig. 18 is a flow chart showing the operation of the first reference voltage generating circuit according to the ninth embodiment of the present invention;

Fig. 19 is a block diagram showing the structure of a clock signal transmitting system according to a tenth embodiment of the present invention;

Fig. 20 is a block diagram showing the structure of a clock signal transmitting system according to an eleventh embodiment of the present invention;

Fig. 21 is a block diagram showing the structure of a clock signal transmitting system according to a twelfth embodiment of the present invention;

Fig. 22 is a block diagram showing the structure of a clock signal transmitting system according to a thirteenth embodiment of the present invention;

Fig. 23 is a block diagram showing the structure of a clock signal transmitting system according to a fourteenth embodiment of the present invention;

Fig. 24 is a block diagram showing the structure of a digital signal transmitting system according to a sixteenth embodiment of the present invention; and

Fig. 25 is a timing diagram showing the timing of the digital signal transmitting system according to the sixteenth embodiment of the present invention.

Description of Preferred Embodiments

Next, with reference to the accompanying drawings, embodiments of the present invention will be explained in detail.

[First Embodiment]

First of all, with reference to Fig. 1, the structure of a clock signal transmitting system according to a first embodiment will be explained.

Referring to Fig. 1, the clock signal transmitting system according to the first embodiment comprises clock signal transmitting circuit 31 and clock signal receiving circuit 32.

Clock signal transmitting circuit 31 comprises controlling circuit 1, first reference voltage generating circuit 2, and first comparator 3. Controlling circuit 1 generates first control signal 14 and second control signal 15. First control signal 14 and second control signal 15 are used to periodically vary first reference voltage 16 and second reference voltage 17, respectively, and to synchronize voltages 16 and 17. First reference voltage generating circuit 2 determines first reference voltage 16 corresponding to first control signal 14 and outputs first reference voltage 16. First comparator 3 inputs source clock signal 11 and first reference voltage 16, compares them, and outputs transmission clock signal 12 whose frequency periodically varies.

Clock signal receiving circuit 32 comprises second reference voltage generating circuit 4 and second comparator 5. Second reference voltage

generating circuit 4 receives second control signal 15 which is supplied from controlling circuit 1 in clock signal transmitting circuit 31 through ransmission path 33, determines second reference voltage 17 corresponding to second control signal 15, and outputs second reference voltage 17.

Second comparator 5 inputs transmission clock signal 12 which is supplied from clock signal transmitting circuit 31 through transmission path 33 and whose frequency periodically varies and second reference voltage 17 which is generated in second reference voltage generating circuit 4, compares transmission clock signal 12 with second reference voltage 17, and outputs reproduced clock signal 13 having a single frequency.

Next, with reference to Figs. 1 and 2, the operation of the clock signal transmitting system according to the first embodiment will be explained.

First, the operation of clock signal transmitting circuit 31 will be explained.

Source clock signal 11 having waveform 101 is input to a + (plus) input terminal of first comparator 3.

First reference voltage 16 having waveform 104 is input to a - (minus) input terminal of first comparator 3. First reference voltage 16 is generated by first reference voltage generating circuit 2. First reference voltage 16 has five voltage levels, that is, VT1, VT2, VT3, VT4, and VT5 (where VT1 < VT2 < VT3 < VT4 < VT5). First reference voltage 16 is in the range of the voltage amplitude of source clock signal 11 which is input to the

+ input terminal of first comparator 3. In this case, the high level voltage of source clock signal 11 is VH1, whereas the low level voltage of source clock signal 11 is VL1. Thus, the relation of VL1 < VT1 < VT2 < VT3 < VT4 < VT5 < VH1 is satisfied.

First reference voltage 16 which is input to first comparator 3 is selected by controlling circuit 1. Controlling circuit 1 generates first control signal 14 in order that first reference voltage 16 varies in the order of VT1, VT2, VT3, VT4, VT5, VT4, VT3, VT2, VT1, VT2, VT3, ... whenever the logical level of source clock signal 11 changes. First control signal 14 designates first reference voltage 16. Alternatively, controlling circuit 1 may generate first control signal 14 at intervals of at least one period of first reference voltage 16. First reference voltage generating circuit 2 autonomously switches first reference voltage 16 in synchronization with first control signal 14. In the latter case, when necessary, first reference voltage generating circuit 2 compensates the phase of first control signal 14.

Next, the operation of first comparator 3 will be explained. At the beginning, first reference voltage generating circuit 2 selects VT1 as first reference voltage 16 corresponding to first control signal 14. When the voltage of source clock signal 11 becomes VT1 (waveform 101) at time T21, first comparator 3 determines that the logical level of source clock signal 11 becomes high and causes the logical level (waveform 102) of transmission clock signal 12 to be high. After first reference voltage generating circuit 2

causes the voltage level of first reference voltage 16 to be raised to VT2, when the voltage level of source clock signal 11 becomes VT2 at time T22, first comparator 3 causes the logical level (waveform 102) of transmission clock signal 12 to be low. Thereafter, because first reference voltage generating circuit 2 varies the voltage level of first reference voltage 16 as represented by waveform 104, first comparator 4 outputs transmission clock signal 12 as represented by waveform 102. It is apparent that frequency of transmission clock signal 12 (waveform 102) periodically varies. The change amount and change period of the frequency of transmission clock signal 12depend on the period of source clock signal 11 and the resolution of first reference voltage 16.

Next, the operation of clock signal receiving circuit 32 will be explained.

A + (plus) input terminal of second comparator 5 inputs transmission clock signal 12 supplied from clock signal transmitting circuit 31 through transmission path 33.

Second reference voltage 17 is input to a - (minus) input terminal of second comparator 5. Second reference voltage 17 is generated by second reference voltage generating circuit 4. Second reference voltage 17 has five voltage levels VT11, VT12, VT13, VT14, and VT15 (where VT11 < VT12 < VT13 < VT14 < VT15). Second reference voltage 17 is in the range of the voltage amplitude of transmission clock signal 12 which is supplied to

second comparator 5. In this case, the voltage of the high level of transmission clock signal 12 is VH2, whereas the voltage of the low level of transmission clock signal 12 is VL2. Thus, the relation of VL2 < VT11 < VT12 < VT13 < VT14 < VT15 < VH2 is satisfied. The number of voltage levels of first reference voltage 16 of clock signal transmitting circuit 31 is the same as the number of voltage levels of second reference voltage 17 of clock signal receiving circuit 32. In addition, as will be explained later, the voltage level of first reference voltage 16 of clock signal transmitting circuit 31 synchronizes with the voltage level of second reference voltage 17 of clock signal receiving circuit 32.

Controlling circuit 1 of clock signal transmitting circuit 31 sends second control signal 15 to second reference voltage generating circuit 4 of clock signal receiving circuit 32. Second control signal 15 contains the synchronization information of first reference voltage 16. Since the phase of first reference voltage 16 is designated by first control signal 14, second control signal 15 also contains the synchronization information of first control signal 14.

For example, even in case first control signal 14 designates first reference voltage 16 whenever first reference voltage 16 should change, controlling circuit 1 only have to send second control signal 15 to second reference voltage generating circuit 4 only when the voltage level of first reference voltage 16 varies from VT1 to VT2. In this case, second reference

voltage generating circuit 4 autonomously switches the voltage level of second reference voltage 17 in synchronization with second control signal 15. When necessary, second reference voltage generating circuit 4 compensates the phase of second reference voltage 17 with respect to second control signal 15.

It is tolerable that the frequency of first control signal 14 sent from controlling circuit 1to first reference voltage generating circuit 2 is twice as high as the frequency of source clock signal 11 from a view point for suppressing electromagnetic noise. However, the frequency of second control signal 15 sent from controlling circuit 1 to second reference voltage generating circuit 4 should be lower than the frequency of source clock signal 11 from a view point for suppressing electromagnetic noise. Second control signal 15 only have to have information at either one of a rising edge or falling edge. Therefore, the duty of second control signal 15 is defined from a view point for suppressing the electromagnetic noise.

However, first control signal 14 and second control signal 15 may be unified into a common control signal. In this case, controlling circuit 1 may generate the common control signal at intervals of at least one period of first reference voltage 16 and second reference voltage 17 and output the common control signal to first reference voltage generating circuit 2 and second reference voltage generating circuit 4. Also in this case, first reference voltage generating circuit 2 and second reference voltage

generating circuit 4 autonomously operate in synchronization with common control signal and in predetermined sequences of voltage levels of the reference voltages, respectively.

As the relation of the first reference voltage of clock signal transmitting circuit 31 and the second reference voltage of tclock signal receiving circuit 32, VT1 corresponds to VT15; VT2 corresponds to VT14; VT3 corresponds to VT13; VT4 corresponds to VT12; and VT5 corresponds to VT11. In other words, the lowest voltage level of first reference voltage 16 of clock signal transmitting circuit 31 corresponds to the highest voltage level of second reference voltage 17 of clock signal receiving circuit 32. The second lowest voltage level of first reference voltage 16 corresponds to the second highest voltage level of second reference voltage 17. The rest of the voltage levels satisfy the same relation. Thus, the relation of VT1 + VT15 = VT2 + VT14 = VT3 + VT13 = VT4 + VT12 = VT5 + VT11 = (a constant voltage) is satisfied. The voltage level of second reference voltage 17 varies in the order of VT15, VT14, VT13, VT12, VT11, VT12, VT13, VT14, VT15, VT14, VT13, and so forth when the logical level of source clock signal 11 changes.

Next, with reference to Fig. 2, the operation of second comparator 5 will be explained. At the beginning, transmission clock signal 12 when VT1 is selected as the voltage level of first reference voltage 16 is transmitted from clock signal transmitting circuit 31 to second comparator 5.

At this point, since VT15 has been selected as the voltage level of the second reference voltage by second reference voltage generating circuit 4, when the voltage level (waveform 102) of transmission clock signal 12 becomes VT15 at time T31, second comparator 5 determines that the logical level of transmission clock signal 12 is high and causes the logical level (waveform 103) of reproduced clock signal 13 to be high. Thereafter, second reference voltage generating circuit 4 varies the voltage level of reference voltage 17 to VT14 corresponding to second control signal 15. After transmission clock signal 12 corresponding to VT2 of first reference voltage 16 is transmitted, when the voltage level of transmission clock signal 12 lowers to VT14 at time T32, second reference voltage generating circuit 4 causes the logical level (waveform 103) of reproduced clock signal 13 to be low. Thereafter, the voltage level of second reference voltage 17 varies as represented by waveform 105, and second comparator 5 outputs reproduced clock signal 13 as represented by waveform 103. The period (the period between rising edges and the period between falling edges) and duty of reproduced clock signal 13 are the same as those of source clock signal 11. In other words, reproduced clock signal 13 having the same waveform 103 as waveform 101 of source clock signal 11 is obtained by clock signal receiving circuit 32.

The voltage levels of first reference voltage 16 and second reference voltage 17 selected in a repetitive period may be any voltages as long as

first reference voltage generating circuit 2 matches second reference voltage generating circuit 4. Although the voltage levels of first reference voltage 16 and second reference voltage 17 vary whenever the logical level of the clock signal changes in the above explanation, they may vary only when the logical level of the clock signal changes several times.

Next, with reference to flow charts as shown in Figs. 3 to 7, the operations of the individual blocks of the first embodiment will be explained.

First, with reference to Fig. 3, the operation of controlling circuit 1 will be explained.

At step S101, ΔT_1, T_C, and N_C are set. ΔT_1 is a time counting unit. T_C is the period in which first control signal 14 is output. N_C is the ratio of the period of second control signal 15 to the period of first control signal 14. At step S102, N is set to 0. N is a variable used to control the period of second control signal 15. At step S103, T is set to 0. T is a variable used to control the period of first control signal 14. At step S104, ΔT_1 is added to T. At step S105, it is determined whether or not T is equal to or greater than T_C. When the determined result at step S105 is Yes, the flow advances to step S106. At step S106, first control signal 14 is output. When the determined result at step S105 is No, the flow returns to step S104. The flow advances from step S106 to step S107. At step S107, N is incremented by 1. At step S108, it is determined whether or not N is equal to N_C. When the determined result at step S108 is Yes, the flow advances

to step S109. At step S109, second control signal 15 is output. When the determined result at step S108 is No, the flow returns to step S103. The flow advances from step S109 to step S110. At step S110, N is reset to 0. Thereafter, the flow returns to step S103. The value of T_C is represented by $T_C = n \times (T_{CLK} / 2)$ (where n is an integer greater than zero; and T_{CLK} is the period of the clock signal). When N is set to 1 at step S101, the period of first control signal 14 is equal to the period of second control signal 15.

Next, with reference to Fig. 4, the operation of the first reference voltage generating circuit 2 will be explained.

At step S201, ΔT_2 is set. ΔT_2 is a time counting unit. Thereafter, at step S202, T is set to 0. T is a variable used to control the time at which the voltage level of first reference voltage 16 is varied. Thereafter, at step S203, it is determined whether or not first control signal 14 has been input. When the determined result at step S203 is Yes, the flow advances to step S207. At step S207, the voltage level of first reference voltage 16 is set to VT1. When the determined result at step S203 is No, the flow advances to step S204. At step S204, ΔT_2 is added to T. Thereafter, at step S205, it is determined whether or not T is equal to or larger than $T_{CLK} / 2$. When the determined result at step S205 is Yes, the flow advances to step S206. At step S206, the voltage level of first reference voltage 16 is varied to the next voltage level in the sequence. Thereafter, the flow returns to step S202. When the determined result at step S205 is No, the flow returns to step

S203.

Next, with reference to Fig. 5, the operation of second reference voltage generating circuit 4 will be explained.

At step S301, ΔT_4 is set. ΔT_4 is a time counting unit. At step S302, T is set to 0. T is a variable used to control the time at which the voltage level of second reference voltage 17 is varied. Thereafter, at step S303, it is determined whether or not second control signal 15 has been input. When the determined result at step S303 is Yes, the flow advances to step S307. At step S307, the voltage level of the first reference voltage 16 is set to VT15. When the determined result at step S303 is No, the flow advances to step S304. At step S304, ΔT_4 is added to T. Thereafter, the flow advances to step S305. At step S305, it is determined whether or not T is equal to or larger than $T_{CLK} / 2$. When the determined result at step S305 is Yes, the flow advances to step S306. At step S306, the voltage level of second reference voltage 17 is varied to the next voltage level in the sequence. Thereafter, the flow returns to step S302. When the determined result at step S305 is No, the flow returns to step S303.

Next, with reference to Fig. 6, the operation of the first comparator 3 will be explained.

At step S401, it is determined whether or not the voltage of source clock signal 11 is equal to or higher than first reference voltage 16. When the determined result at step S401 is Yes, the flow advances to step S402.

When the determined result at step S401 is No, the flow advances to step S403. At step S402, the logical level of transmission clock signal 12 is set to high. Thereafter, the flow returns to step S401. At step S403, the logical level of transmission clock signal 12 is set to low. Thereafter, the flow returns to step S401.

Next, with reference to Fig. 7, the operation of second comparator 5 will be explained.

At step S501, it is determined whether or not the voltage of the transmission clock signal 12 is equal to or higher than second reference voltage 17. When the determined result at step S501 is Yes, the flow advances to step S502. When the determined result at step S501 is No, the flow advances to step S503. At step S502, the logical level of reproduced clock signal 13 is set to high. Thereafter, the flow returns to step S501. At step S503, the logical level of reproduced clock signal 13 is set to low. Thereafter, the flow returns to step S501.

[Second Embodiment]

According to a second embodiment of the present invention shown in Fig. 8, controlling circuit 1 inputs source clock signal 11 and detects the timing at which the voltage level of the waveform of source clock signal 11 becomes VH1 and the timing at which the voltage level of the waveform of source clock signal 11 becomes VL1. Corresponding to these timings, controlling circuit 1 generates first control signal 14 and second control

signal 15. This operation is based on the principle that when the voltage level of source clock signal 11 is varied, the voltage levels of first reference voltage 16 and second reference voltage 17 should be varied. First control signal 14 is output whenever the voltage level of the waveform of source clock signal 11 becomes VH1 or VL1. Alternatively, first control signal 14 is output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse. Second control signal 15 is output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse. First control signal 14 and second control signal 15 may be unified. In this case, first reference signal 14 and second control signal 15 are simultaneously output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse.

Next, with reference to Figs. 9A, 9B, and 10, the structure and the operation of controlling circuit 1 according to the second embodiment of the present invention will be explained.

The timings at which the voltage level of the waveform of source clock signal 11 becomes VH1 and VL1 are detected by supplying source clock signal 11 to a circuit shown in Fig. 9A and observing the timing at which the logical level of a change detection signal becomes high. Fig. 9B shows waveforms of the input signal of the circuit shown in Fig. 9A and the change detection signal.

Referring to Fig. 10, at step S601, M_C and N_C are set. M_C represetnts

the ratio of the period of first control signal 14 to the period of the clock signal. N_C represents the ratio of the period of second control signal 15 to the period of first control signal 14. Thereafter, at step S602, N is set to 0. N is a variable used to control the period of first control signal 14. Thereafter, at step S603, M is set to 0. M is a variable used to control the period of second control signal 15. Thereafter, at step S604, it is determined whether or not the change detecting signal has been output from the circuit shown in Fig. 9A. When the determined result at step S604 is Yes, the flow advances to step S605. When the determined result at step S604 is No, the flow returns to step S604. At step S605, M is incremented by 1. Thereafter, at step S606, it is determined whether or not M is equal to M_C. When the determined result at step S606 is Yes, the flow advances to step S607. when the determined result at step S606 is No, the flow returns to step S604. At step S607, the first control signal is output. Thereafter, at step S608, N is incremented by 1. Thereafter, at step S609, it is determined whether or not N is equal to N_C. When the determined result at step S609 is Yes, the flow advances to step S610. When the determined result at step S609 is No, the flow returns to step S603. At step S610, the second control signal is output. Thereafter, at step S611, N is set to 0. Thereafter, the flow returns to step S603.

[Third Embodiment]

According to a third embodiment of the present invention shown in

Fig. 11, controlling circuit 1 inputs transmission clock signal 12, detects the timings at which the voltage level of the waveform of transmission clock signal 12 becomes VH2 and the timings at which the voltage level of the waveform of transmission clock signal 12 becomes VL2, and generates first control signal 14 and second control signal 15 corresponding to these detection timings. This operation is based on the principle that when the voltage level of transmission clock signal 12 is varied, the voltage level of the second reference voltage 17 may be varied and the voltage level of first reference voltage 16 may be varied. It is not too late to vary the voltage of first reference voltage 16 when the voltage level of transmission clock signal 12 is changed. First control signal 14 is output whenever the voltage level of the waveform of source clock signal 11 becomes VH1 or VL1. Alternatively, first control signal 14 is output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse. Second control signal 15 is output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse. First control signal 14 and second control signal 15 may be unified. In this case, first reference signal 14 and second control signal 15 are simultaneously output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse.

Since the structure and operation of the controlling circuit 1 according to the third embodiment are the same as those according to the

second embodiment (see Figs. 9 and 10), the redundant description is omitted.

[Fourth Embodiment]

According to a fourth embodiment of the present invention shown in Fig. 12, controlling circuit 1 inputs source clock signal 11 and transmission clock signal 12, detects the timings at which the voltage level of the waveform of source clock signal 11 becomes VH1 and timings at which the voltage level of the waveform of source clock signal 11 becomes VL1, generates first control signal 14 corresponding to the detection timings, detects the timings at which the voltage level of the waveform of transmission clock signal 12 becomes VH2 and timings at which the voltage level of the waveform of transmission clock signal 12 becomes VL2, and generates second control signal 15 corresponding to the detection timings. This operation is based on the principle that when the voltage level of source clock signal 11 is varied, the voltage level offirst reference voltage 16 can be varied, and when the voltage level of transmission clock signal 12 is varied, the voltage level of first reference voltage 16 can be varied. First control signal 14 is output whenever the voltage level of the waveform of source clock signal 11 becomes VH1 or VL1. Alternatively, first control signal 14 is output every time when one or more period of first reference voltage 16 and second reference voltage 17 elapse. Second control signal 15 is output every time when one or more period of first reference voltage 16

and second reference voltage 17 elapse.

Since the structure and operation of the controlling circuit 1 according to the fourth embodiment of the present invention are the same as those according to the second embodiment, the redundant description is omitted.

Controlling circuit 1 may generates first control signal 14 and second control signal 15 at the timing at which the logical level of source clock signal 11 becomes identical with the logical level of transmission clock signal 12. In this case, similarly to the second embodiment and the third embodiment, first control signal 14 and second control signal 15 may be unified.

[Fifth Embodiment]

According to a fifth embodiment of the present invention shown in Fig. 13, a PLL 6 is disposed. Thus, clock signal receiving circuit 32B is used in the place of clock signal receiving circuit 32. PLL 6 inputs reproduced clock signal 13 as a reference signal from second comparator 5 to output reproduced clock signal 13B. The fifth embodiment is used when high accuracy of the frequency of the clock signal is required. Since certain accuracy of the frequency of reproduced clock signal 13 is obtained, a conventional PLL may be used as PLL 6.. Thus, a reproduced clock signal with desired accuracy can be obtained without need to use a complicated PLL circuit which compensates the frequency fluctuation of several percent.

[Sixth Embodiment]

Since there is a phase difference between source clock signal 11 and reproduced clock signal 13, phase compensating circuit 7 as shown in Fig. 14 may be disposed at the following stage of the second comparator 5 in order to have the phase difference of reproduced clock signal 13 to a data signal (not shown) be equal to the phase difference of source clock signal 11 to the data signal (not shown).

[Seventh Embodiment]

In order to attain the same purpose as the sixth embodiment, as shown in Fig. 15, phase compensating circuit 7 may be disposed between second comparator 5 and PLL 6.

[Eighth Embodiment]

In order to attain the same purpose as the sixth embodiment, as shown in Fig. 16, phase compensating circuit 7 may be disposed at the following stage of PLL 6.

[Ninth Embodiment]

According to a ninth embodiment of the present invention shown in Fig. 17, controlling circuit 1 outputs first control signal 14 to first reference voltage generating circuit 2 every time when one or more periods of first reference voltage 16 and second reference voltage 17 elapse. First reference voltage generating circuit 2 inputs source clock signal 11 and first control signal 14 and causes a built-in flywheel circuit to use source clock

signal 11 as a clock signal and first control signal 14 as a phase synchronization signal so as to generate first reference voltage 16.

Next, with reference to Fig. 18, the operation of first reference voltage generating circuit 2 according to the ninth embodiment will be explained.

Referring to Fig. 18, at step S701, it is determined whether or not first control signal 14 has been input. When the determined result at step S701 is Yes, the flow advances to step S704. At step S704, the voltage level of first reference voltage 16 is set to VT1. When the determined result at step S701 is No, the flow advances to step S702. At step S702, it is determined whether or not the change detection signal has been output from the circuit shown in Fig. 9 included in first reference voltage generating circuit 2. When the determined result at step S702 is Yes, the flow advances to step S703. At step S703, the voltage level of the first reference voltage is varied to the next voltage level in the sequence. When the determined result at step S702 is No, the flow returns to step S701.

[Tenth Embodiment]

According to a tenth embodiment of the present invention shown in Fig. 19, controlling circuit 1 outputs first control signal 14 to first reference voltage generating circuit 2 every time when one or more periods of first reference voltage 16 and second reference voltage 17 elapse. First reference voltage generating circuit 2 inputs transmission clock signal 12 and first control signal 14 and causes a built-in flywheel circuit to use

transmission clock signal 12 as a clock signal and first control signal 14 as a phase synchronization signal so as to generate first reference voltage 16.

Since the operation of first reference voltage generating circuit 2 according to the tenth embodiment is the same as that according to the ninth embodiment (see Fig. 18), the redundant description is omitted.

[Eleventh Embodiment]

According to an eleventh embodiment of the present invention shown in Fig. 20, controlling circuit 1 outputs second control signal 15 to second reference voltage generating circuit 4 every time when one or more periods of first reference voltage 16 and the second reference voltage 17 elapse. Second reference voltage generating circuit 4 inputs transmission clock signal 12 and second control signal 15 and causes a built-in flywheel circuit to use transmission clock signal 12 as a clock signal and second control signal 15 as a phase synchronization signal so as to generate second reference voltage 17.

Since the operation of second reference voltage generating circuit 4 according to the eleventh embodiment is the same as the operation of first reference voltage generating circuit 2 according to the ninth embodiment (see Fig. 18), the redundant description is omitted.

[Twelfth Embodiment]

According to a twelfth embodiment of the present invention shown in Fig. 21, controlling circuit 1 outputs second control signal 15 to second

reference voltage generating circuit 4 every time when one or more periods of first reference voltage 16 and second reference voltage 17 elapse. Second reference voltage generating circuit 4 inputs reproduced clock signal 13 and second control signal 15 and causes a built-in flywheel circuit to use reproduced clock signal 13 as a clock signal and second control signal 15 as a phase synchronization signal so as to generate second reference voltage 17.

Since the operation of second reference voltage generating circuit 4 according to the twelfth embodiment is the same as the operation of first reference voltage generating circuit 2 according to the ninth embodiment (see Fig. 18), the redundant description is omitted.

[Thirteenth Embodiment]

According to a thirteenth embodiment of the present invention shown in Fig. 22, controlling circuit 1 outputs second control signal 15 to second reference voltage generating circuit 4 every time when one or more periods of first reference voltage 16 and second reference voltage 17 elapse. Local oscillator 8 outputs local clock signal 18 to second reference voltage generating circuit 4. Second reference voltage generating circuit 4 inputs local clock signal 18 and second control signal 15 and causes a built-in flywheel to use local clock signal 18 as a clock signal and second control signal 15 as a phase synchronization signal so as to generate second reference voltage 17.

Since the operation of second reference voltage generating circuit 4

according to the thirteenth embodiment is the same as the operation of first reference voltage generating circuit 2 according to the ninth embodiment (see Fig. 18), the redundant description is omitted.

[Fourteenth Embodiment]

According to a fourteenth embodiment of the present invention shown in Fig. 23, controlling circuit 1 outputs second control signal 15 to second reference voltage generating circuit 4 every time when one or more periods of first reference voltage 16 and second reference voltage 17 elapse. Second reference voltage generating circuit 4 inputs reproduced clock signal 13B and second control signal 15 and causes a built-in flywheel circuit to use reproduced clock signal 13B as a clock signal and second control signal 15 as a phase synchronization signal so as to generate second reference voltage 17.

Since the operation of second reference voltage generating circuit 4 according to the fourteenth embodiment is the same as the operation of first reference voltage generating circuit 2 according to the ninth embodiment (see Fig. 18), the redundant description is omitted.

[Fifteenth Embodiment]

Since the second to fourth embodiments, the ninth and tenth embodiments, and the eleventh to fourteenth embodiments can be freely combined, 24 modifications ($3 \times 2 \times 4 = 24$) can be accomplished.

[Sixteenth Embodiment]

Fig. 24 shows the structure of a digital signal transmitting system

according to a sixteenth embodiment of the present invention. Referring to Fig. 24, according to the sixteenth embodiment, third comparator 9 and fourth comparator 10 are added to the structure of the first embodiment shown in Fig. 1. Third comparator 9 and fourth comparator 10 are used to transmit a data signal. Third comparator 9 inputs first reference voltage 16 and source data signal 21, compares them, and outputs the compared result as transmission data signal 22. Fourth comparator 10 inputs second reference voltage 17 and transmission data signal 22, compares them, and outputs the compared result as reproduced data signal 23.

Fig. 25 is a timing diagram showing waveform 201 of source data signal 21, waveform 202 of transmission data signal 22, waveform 203 of reproduced data signal 23, waveform 104 of first reference voltage 16, and waveform 105 of second reference voltage 17. Referring to Fig. 25, although the timing of the rising edge of transmission data signal 22 is not simultaneous with the timing of the falling edge of transmission data signal 22, the timing the of rising edge of the reproduced data signal 23 is simultaneous with the timing of the falling edge of reproduced data signal 23.

In other words, when the logical level of source data signal 21 becomes high, the waveform 202 of transmission data signal 22 begins to rise at times T21, T23, T25, T27, and T29. When the logical level of transmission data signal 22 becomes high, the waveform 203 of reproduced

data signal 23 begins to rise at times T31, T33, T35, T37, and T39. On the other hand, when the logical level of source data signal 21becomes low, waveform 202 of the logical level of transmission data signal 22 begins to fall at times T41, T23, T43, T27, and T45. When the logical level of transmission data signal 22 becomes low, the waveform 203 of reproduced data signal 23 begins to fall at times T31, T33, T35, T37, and T39.

Thus, although the phase of reproduced data signal 23 is delayed from the phase of source data signal 21, the waveform of reproduced data signal 23 becomes identical with the waveform of source data signal 21. In other words, jitters contained in the transmission data signal 22 is removed from reproduced data signal 23.

It should be noted that the second to fifteenth embodiments can be applied to the sixteenth embodiment as their modifications.

As was explained above, according to the present invention, since a source clock signal and a first reference voltage that periodically varies are input to a first comparator, the frequency of a transmission clock signal can be periodically varied corresponding to the timings at which the logical level of the clock signal becomes high and low. Thus, electromagnetic noise which takes place upon transmission of the transmission clock signal can be suppressed. This effect applies to a data signal.

Synchronization information of a control signal on a transmission side of a transmission clock signal is transmitted to a clock signal receiving

circuit. Corresponding to the synchronous signal, a second reference voltage is periodically varied. Thus, a reproduced clock signal having a single frequency is obtained from a transmission clock signal whose frequency periodically varies. This effect applies to a data signal.

Although the present invention has been shown and explained with respect to the best modes of embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail thereof may be made therein without departing from the spirit and scope of the present invention.

What is claimed is:

1. A clock signal transmitting system, comprising:

a controlling circuit for generating a first control signal and a second control signal which contains synchronization information of said first control signal;

a first reference voltage generating circuit for generating a first reference voltage which periodically varies corresponding to said first control signal;

a second reference voltage generating circuit for generating a second reference voltage which periodically varies corresponding to said second control signal;

a first comparator for comparing a source clock signal with said first reference voltage in order to generate a transmission clock signal; and

a second comparator for comparing said transmission clock signal with said second reference voltage in order to generate a reproduced clock signal.

2. The clock signal transmitting system as set forth in claim 1, wherein the sum of said first reference voltage generated by said first reference voltage generating circuit and said second reference voltage generated by said second reference voltage generating circuit is a constant voltage.

3. The clock signal transmitting system as set forth in claim 1, wherein said first reference voltage generated by said first reference voltage generating circuit and said second reference voltage generated by said second reference voltage generating circuit periodically vary in the same period.

4. The clock signal transmitting system as set forth in claim 1, wherein said first reference voltage generating circuit switches said first reference voltage at a frequency twice as high as said source clock signal, and

wherein said second reference voltage generating circuit switches said second reference voltage at the frequency twice as high as said source clock signal.

5. The clock signal transmitting system as set forth in claim 1, wherein said controlling circuit is disposed on a transmission side.

6. The clock signal transmitting system as set forth in claim 5, wherein said controlling circuit generates said first control signal and said second control signal on the basis of said source clock signal.

7. The clock signal transmitting system as set forth in claim 5, wherein said controlling circuit generates said first control signal and said second control signal on the basis of said transmission clock signal.

8. The clock signal transmitting system as set forth in claim 5, wherein said controlling circuit generates said first control signal and said second control signal on the basis of said source clock signal and said transmission clock signal.

9. The clock signal transmitting system as set forth in claims 1, wherein said controlling circuit generates said second control signal having a frequency which is lower than a frequency of said source clock signal.

10. The clock signal transmitting system as set forth in claim 1, wherein said first reference voltage generating circuit generates said first reference voltage on the basis of said first control signal and said source clock signal.

11. The clock signal transmitting system as set forth in claim 1, wherein said first reference voltage generating circuit generates said first reference voltage on the basis of said first control signal and said

transmission clock signal.

12. The clock signal transmitting system as set forth in claim 1, wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said transmission clock signal.

13. The clock signal transmitting system as set forth in claims 1, wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said reproduced clock signal.

14. The clock signal transmitting system as set forth in claim 1, further comprising:

a local oscillator disposed on a reception side for generating a local clock signal,

wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said local clock signal.

15. The clock signal transmitting system as set forth in claim 1, further comprising:

a PLL circuit which inputs said reproduced clock signal as a reference signal in order to output a refined reproduced clock signal.

16. The clock signal transmitting system as set forth in claim 1, further comprising:

a PLL circuit which inputs said reproduced clock signal as a reference signal in order to output a refined reproduced signal,

wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said refined reproduced signal.

17. The clock signal transmitting system as set forth in claim 1, further comprising:

a phase compensating circuit for compensating the phase of said reproduced clock signal.

18. The clock signal transmitting system as set forth in claim 1,

wherein said first control signal is the same as said second control signal.

19. A digital signal transmitting system, comprising:

the clock transmitting system as set forth in claim 1;

a third comparator for comparing a source data signal with said first reference voltage in order to generate a transmission data signal; and

a fourth comparator for comparing said transmission data signal with said second reference voltage in order to generate a reproduced data signal.

20. A clock signal transmitting method, comprising the steps of:

(a) generating a first control signal and a second control signal which contains synchronization information of said first control signal;

(b) generating a first reference voltage which periodically varies corresponding to said first control signal;

(c) generating a second reference voltage which periodically varies corresponding to said second control signal;

(d) comparing a source clock signal with said first reference voltage in order to generate a transmission clock signal; and

(e) comparing said transmission clock signal with said second reference voltage in order to generate a reproduced clock signal.

21. The clock signal transmitting method as set forth in claim 20, wherein the sum of said first reference voltage generated at the first reference voltage generating step (b) and said second reference voltage generated at the second reference voltage generating step (c) is a constant voltage.

22. The clock signal transmitting method as set forth in claim 20, wherein said first reference voltage generated at the first reference voltage generating step (b) and said second reference voltage generated at the second reference voltage generating step (c) periodically vary in the same period.

23. The clock signal transmitting method as set forth in claim 20, wherein the first reference voltage generating step (b) is performed by switching said first reference voltage at a frequency twice as high as said source clock signal, and

wherein the second reference voltage generating step (c) is performed by switching said second reference voltage at the frequency twice as high as said source clock signal.

24. The clock signal transmitting method as set forth in claim 20, wherein the first and second control signals generating step (a) is performed on a transmission side.

25. The clock signal transmitting method as set forth in claim 24, wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control

signal on the basis of said source clock signal.

26. The clock signal transmitting method as set forth in claim 24, wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control signal on the basis of said transmission clock signal.

27. The clock signal transmitting method as set forth in claim 24, wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control signal on the basis of said source clock signal and said transmission clock signal.

28. The clock signal transmitting method as set forth in claim 20, wherein the first and second control signals generating step (a) is performed by generating said second control signal having a frequency which is lower than a frequency of said source clock signal.

29. The clock signal transmitting method as set forth in claim 20, wherein the first reference voltage generating step (b) is performed by generating said first reference voltage on the basis of said first control signal and said source clock signal.

30. The clock signal transmitting method as set forth in claim 20, wherein the first reference voltage generating step (b) is performed by generating said first reference voltage on the basis of said first control signal and said transmission clock signal.

31. The clock signal transmitting method as set forth in claim 20, wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said transmission clock signal.

32. The clock signal transmitting method as set forth in claim 20, wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said reproduced clock signal.

33. The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(f) generating a local clock signal on a reception side,

wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said local clock signal.

34. The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(g) supplying said reproduced clock signal as a reference signal to a PLL circuit in order to obtain a refined reproduced clock signal from said PLL circuit.

35. The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(h) supplying said reproduced clock signal as a reference signal to a PLL circuit in order to obtain a refined reproduced clock signal from said PLL circuit,

wherein said second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said refined reproduced clock signal.

36. The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(i) compensating the phase of said reproduced clock signal.

37. The clock signal transmitting method as set forth in claim 20, wherein said first control signal is the same as said second control

signal.

38. A digital signal transmitting method, comprising the steps of:

the clock transmitting method as set forth in claim 20;

(j) comparing a source data signal with said first reference voltage in order to generate a transmission data signal; and

(k) comparing said transmission data signal with said second reference voltage in order to generate a reproduced data signalq.

Abstract of the Disclosure

A clock signal transmitting system is disclosed, which comprises a controlling circuit for generating a first control signal and a second control signal which contains synchronization information of the first control signal, a first reference voltage generating circuit for generating a first reference voltage which periodically varies corresponding to the first control signal, a second reference voltage generating circuit for generating a second reference voltage which periodically varies corresponding to the second control signal, a first comparator for comparing a source clock signal with the first reference voltage and generating a transmission clock signal, and a second comparator for comparing the transmission clock signal with the second reference voltage and generating a reproduced clock signal.

FIG. 1

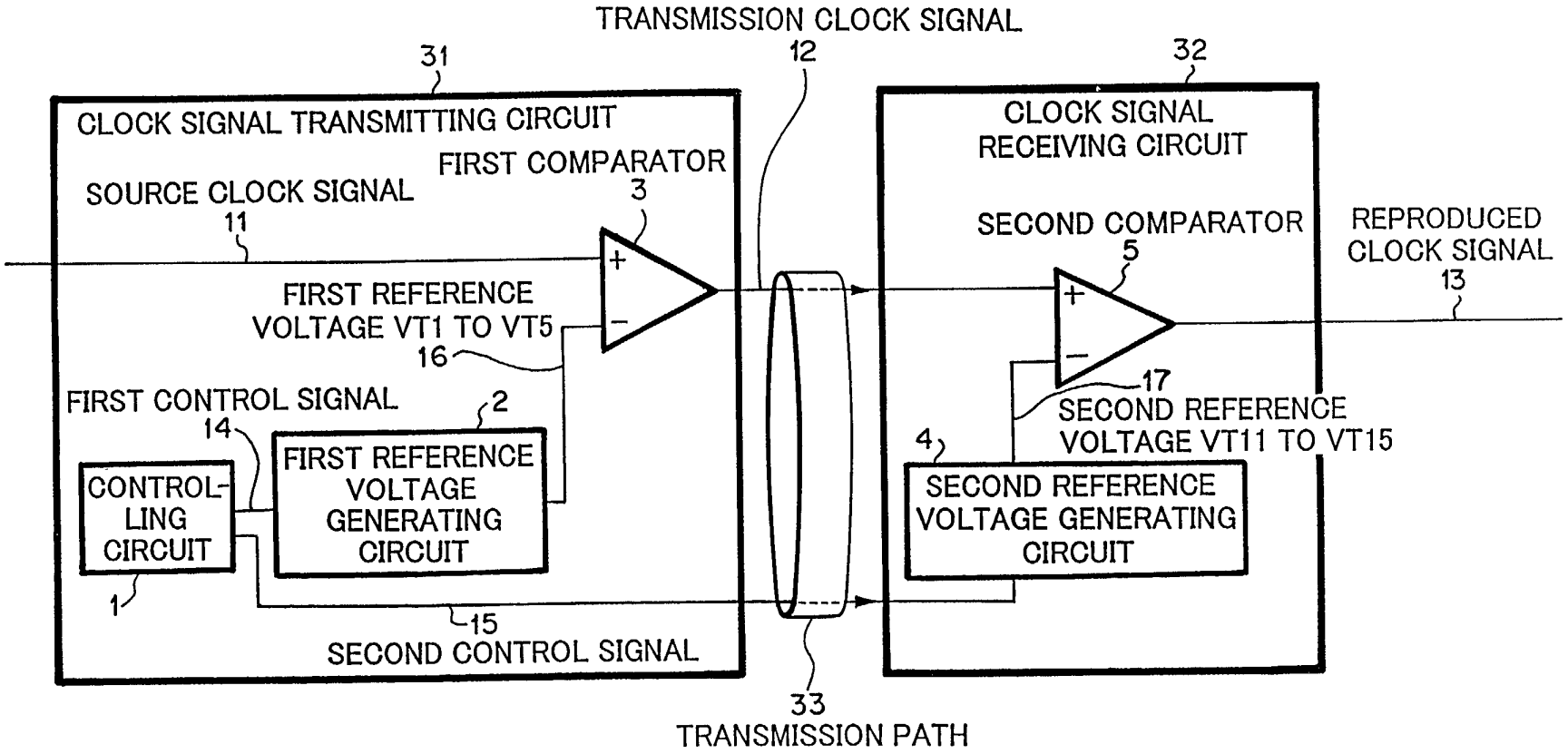

TRANSMISSION CLOCK SIGNAL
31
12
32
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
FIRST CONTROL SIGNAL
2
14
4
CONTROL-LING CIRCUIT
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
1
15
SECOND CONTROL SIGNAL
33
TRANSMISSION PATH

FIG. 2

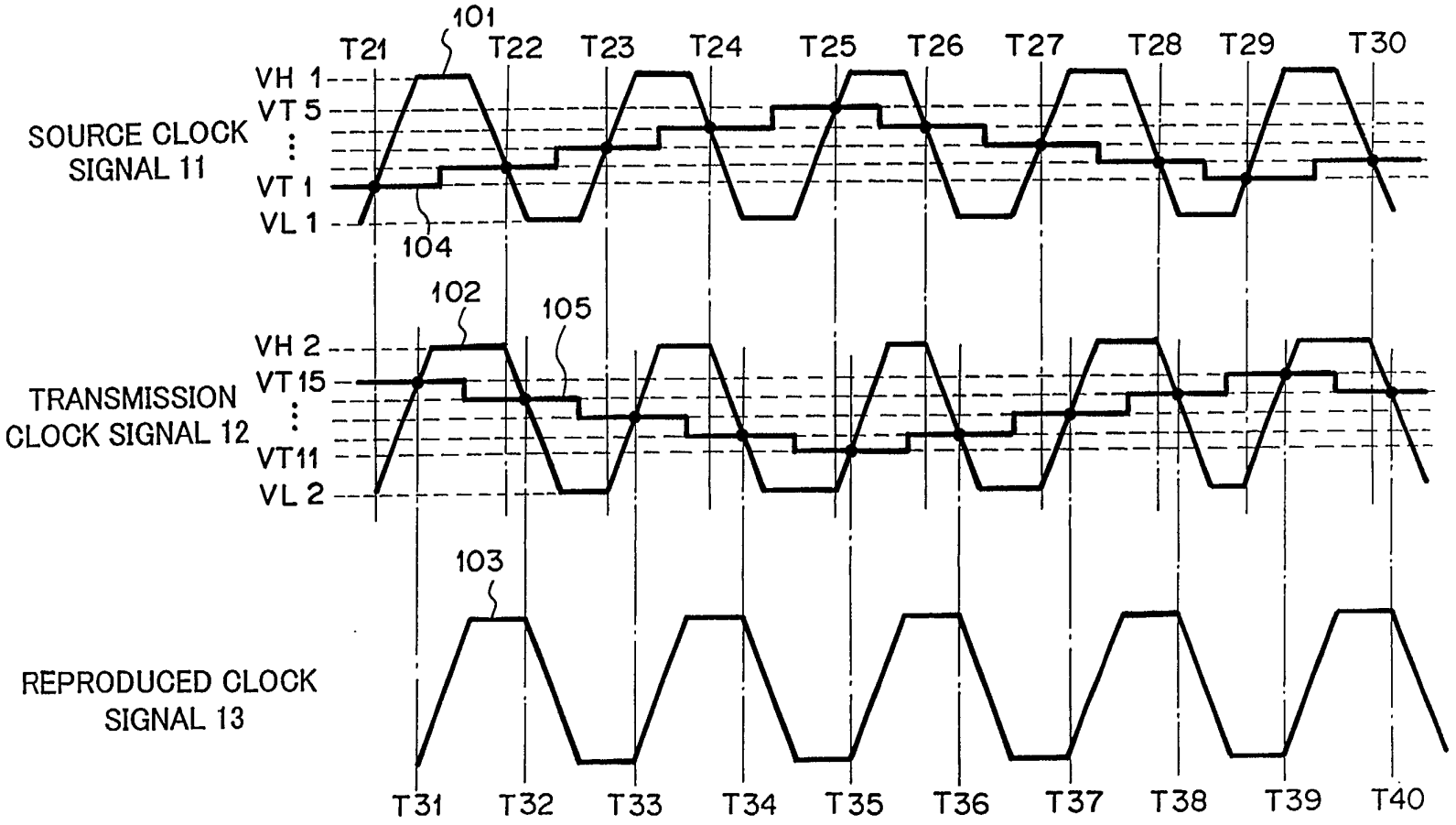

101
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
VH 1
VT 5
VT 1
VL 1
SOURCE CLOCK SIGNAL 11
104
102
105
VH 2
VT15
VT11
VL 2
TRANSMISSION CLOCK SIGNAL 12
103
REPRODUCED CLOCK SIGNAL 13
T31
T32
T33
T34
T35
T36
T37
T38
T39
T40

FIG. 3

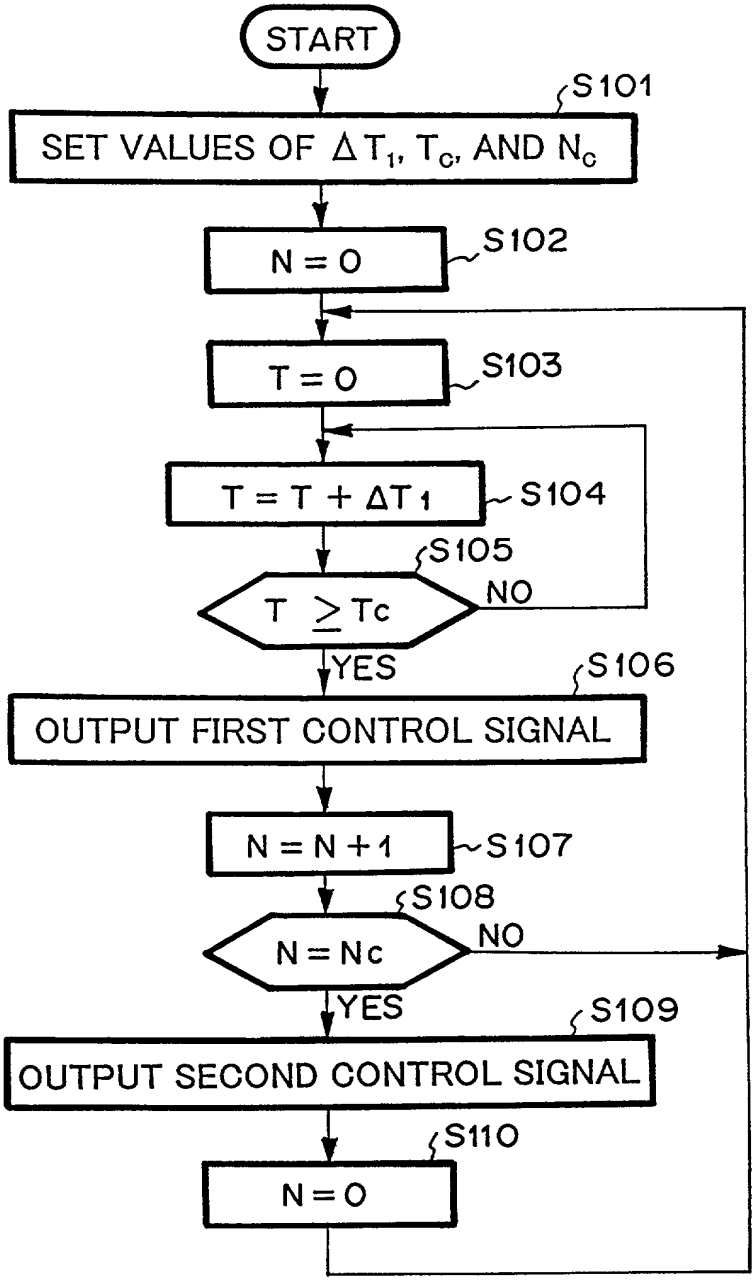

START
S101
SET VALUES OF ΔT1, Tc, AND Nc
N = 0
S102
T = 0
S103
T = T + ΔT1
S104
S105
T ≥ Tc
NO
YES
S106
OUTPUT FIRST CONTROL SIGNAL
N = N + 1
S107
S108
N = Nc
NO
YES
S109
OUTPUT SECOND CONTROL SIGNAL
S110
N = 0

FIG. 4

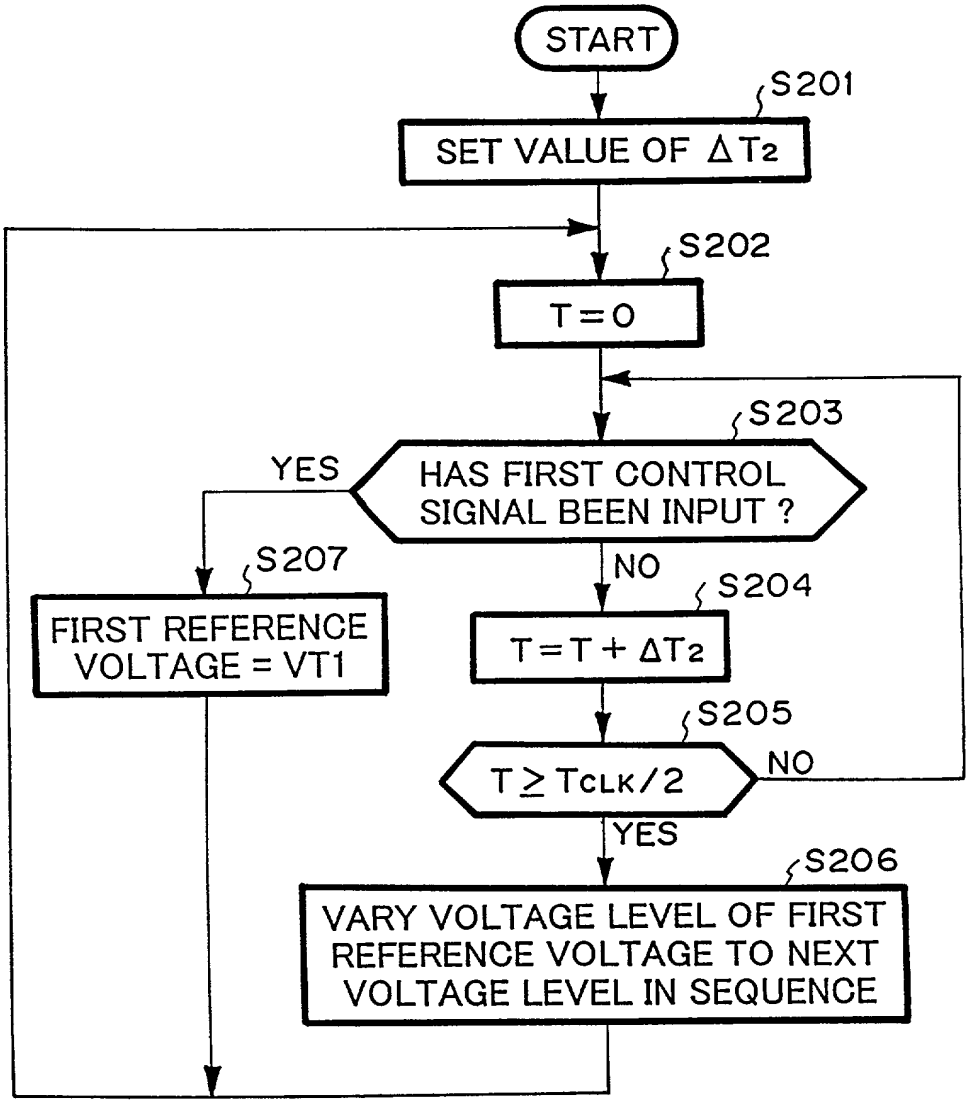

START
S201
SET VALUE OF ΔT2
S202
T=0
S203
HAS FIRST CONTROL SIGNAL BEEN INPUT ?
YES
NO
S207
FIRST REFERENCE VOLTAGE = VT1
S204
T=T+ΔT2
S205
T≥TCLK/2
NO
YES
S206
VARY VOLTAGE LEVEL OF FIRST REFERENCE VOLTAGE TO NEXT VOLTAGE LEVEL IN SEQUENCE

FIG. 5

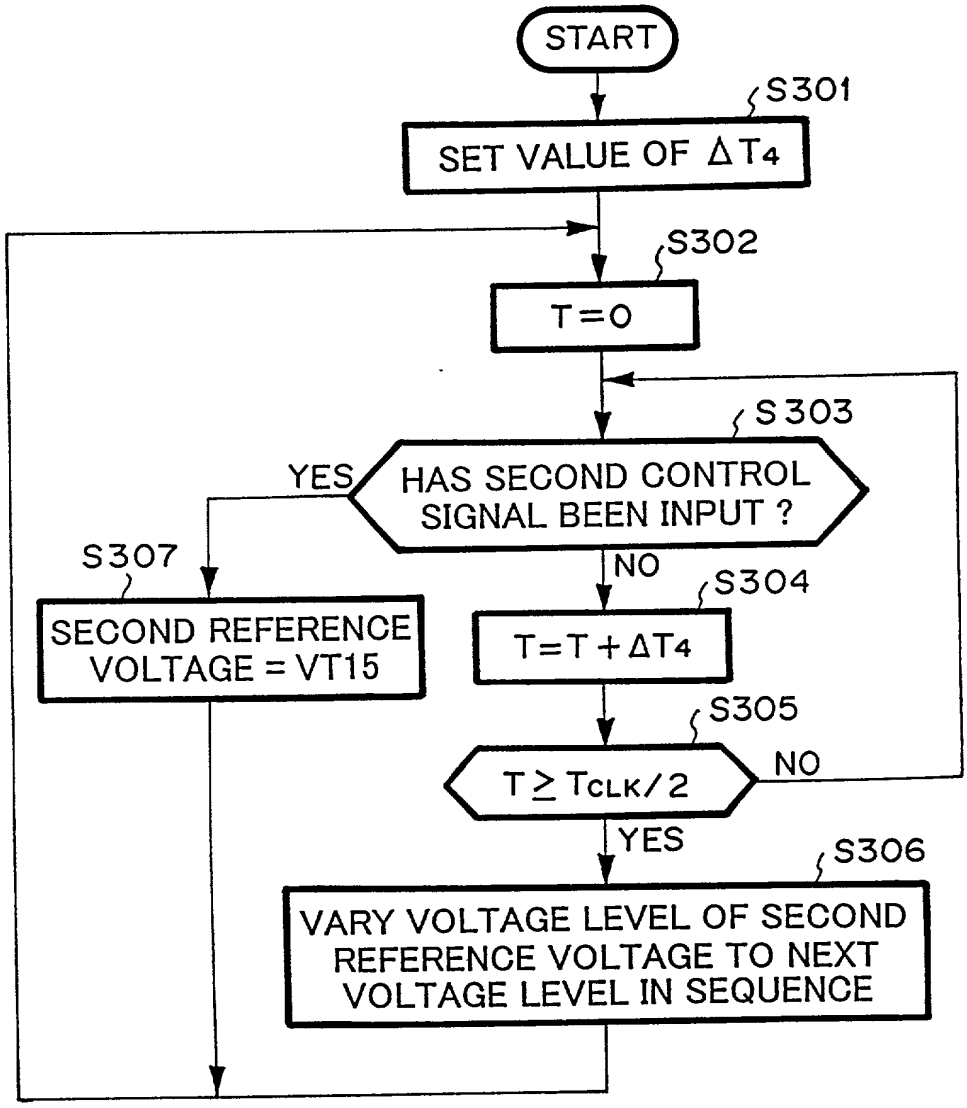

START
S301
SET VALUE OF ΔT4
S302
T=0
S303
HAS SECOND CONTROL SIGNAL BEEN INPUT ?
YES
NO
S307
SECOND REFERENCE VOLTAGE = VT15
S304
T=T+ΔT4
S305
T≥TCLK/2
NO
YES
S306
VARY VOLTAGE LEVEL OF SECOND REFERENCE VOLTAGE TO NEXT VOLTAGE LEVEL IN SEQUENCE

FIG. 6

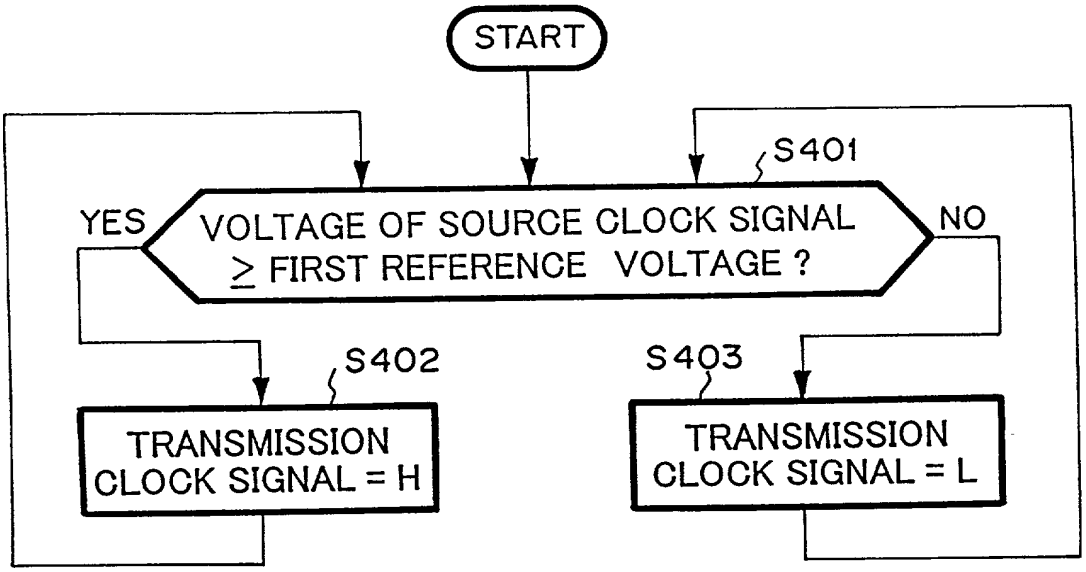

START
S401
YES
VOLTAGE OF SOURCE CLOCK SIGNAL ≥ FIRST REFERENCE VOLTAGE ?
NO
S402
TRANSMISSION CLOCK SIGNAL = H
S403
TRANSMISSION CLOCK SIGNAL = L

FIG. 7

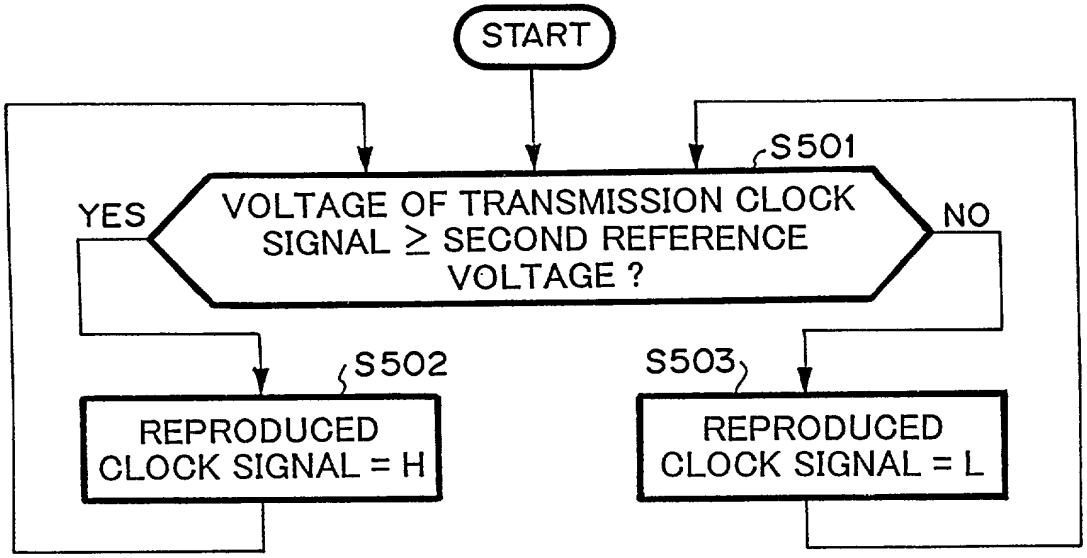
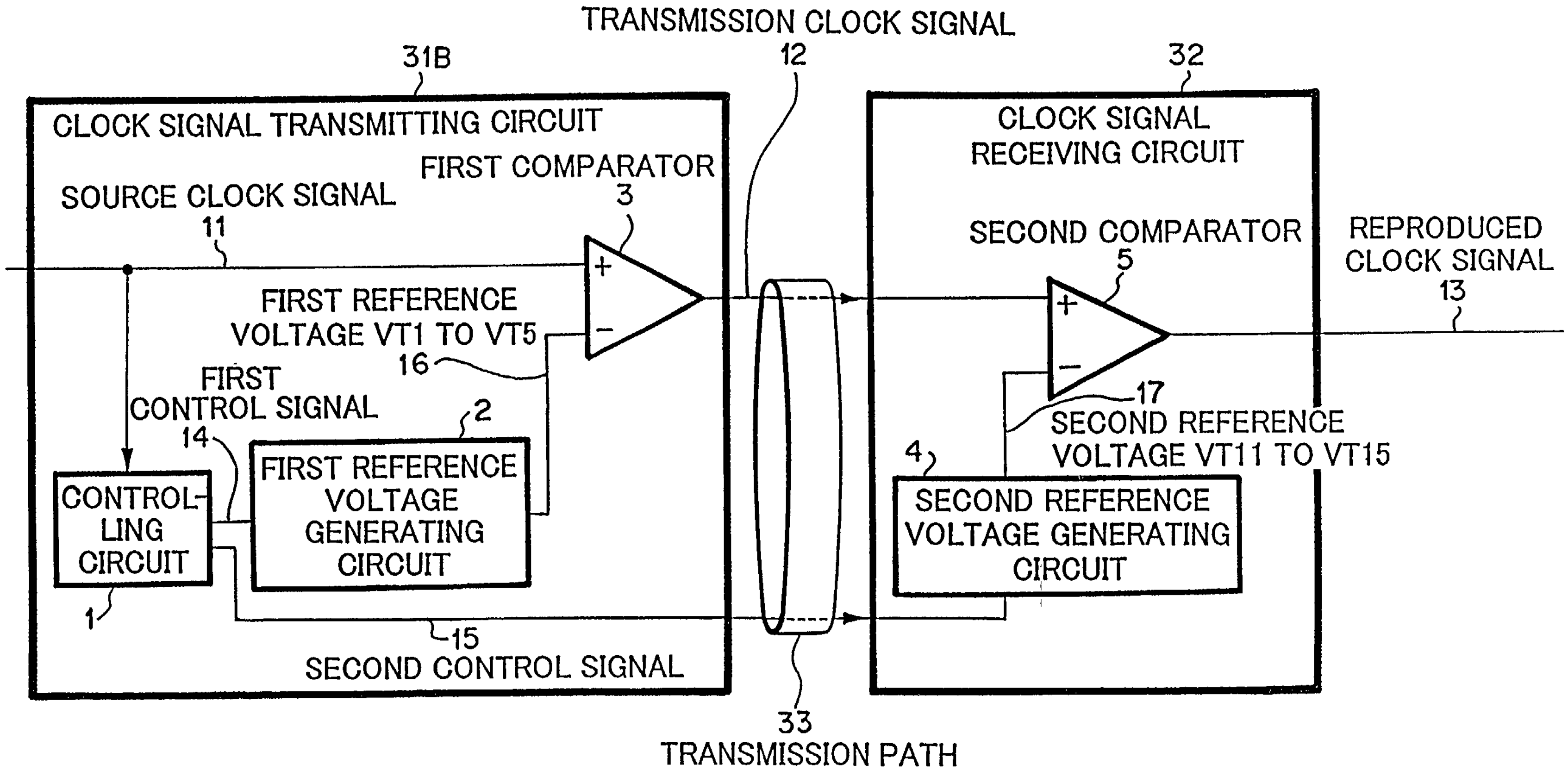
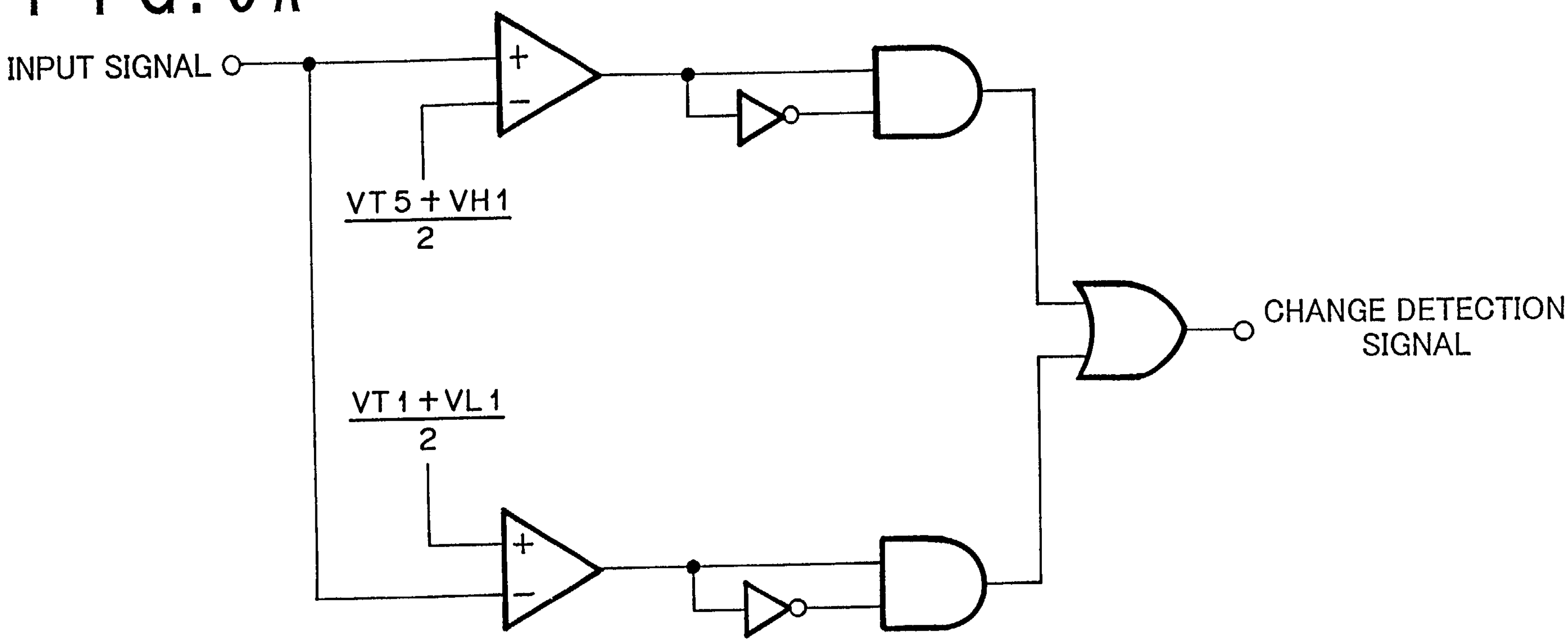

START
S501
YES
VOLTAGE OF TRANSMISSION CLOCK SIGNAL ≥ SECOND REFERENCE VOLTAGE ?
NO
S502
REPRODUCED CLOCK SIGNAL = H
S503
REPRODUCED CLOCK SIGNAL = L

FIG. 8



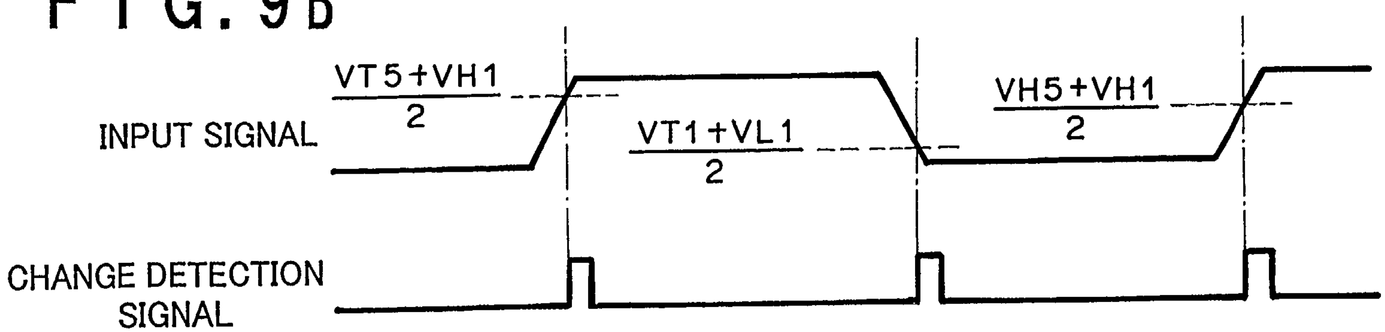
TRANSMISSION CLOCK SIGNAL
12
31B
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE
VOLTAGE VT1 TO VT5
16
FIRST
CONTROL SIGNAL
14
2
FIRST REFERENCE
VOLTAGE
GENERATING
CIRCUIT
CONTROL-
LING
CIRCUIT
1
15
SECOND CONTROL SIGNAL
32
CLOCK SIGNAL
RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED
CLOCK SIGNAL
13
17
SECOND REFERENCE
VOLTAGE VT11 TO VT15
4
SECOND REFERENCE
VOLTAGE GENERATING
CIRCUIT
33
TRANSMISSION PATH

F I G. 9 A



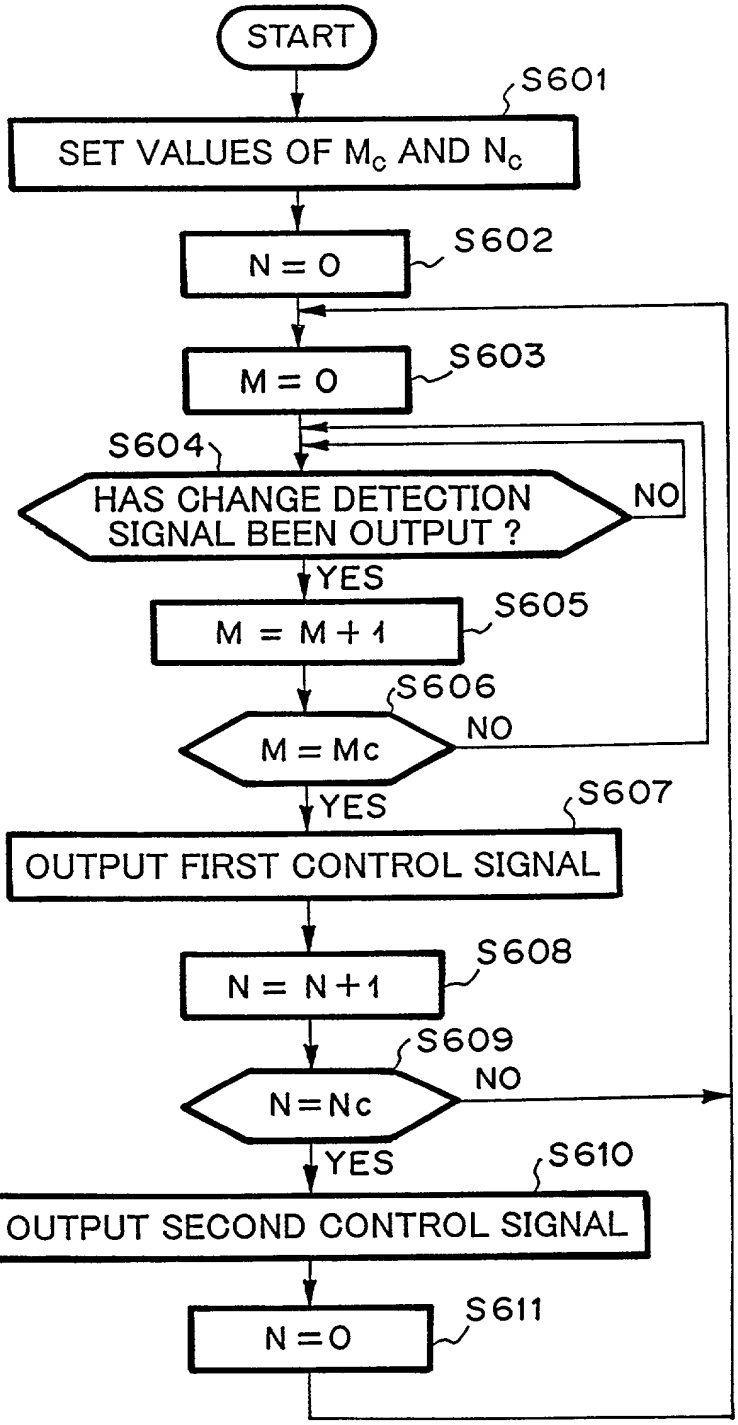
INPUT SIGNAL
VT5 + VH1 / 2
VT1 + VL1 / 2
CHANGE DETECTION SIGNAL

F I G. 9 B

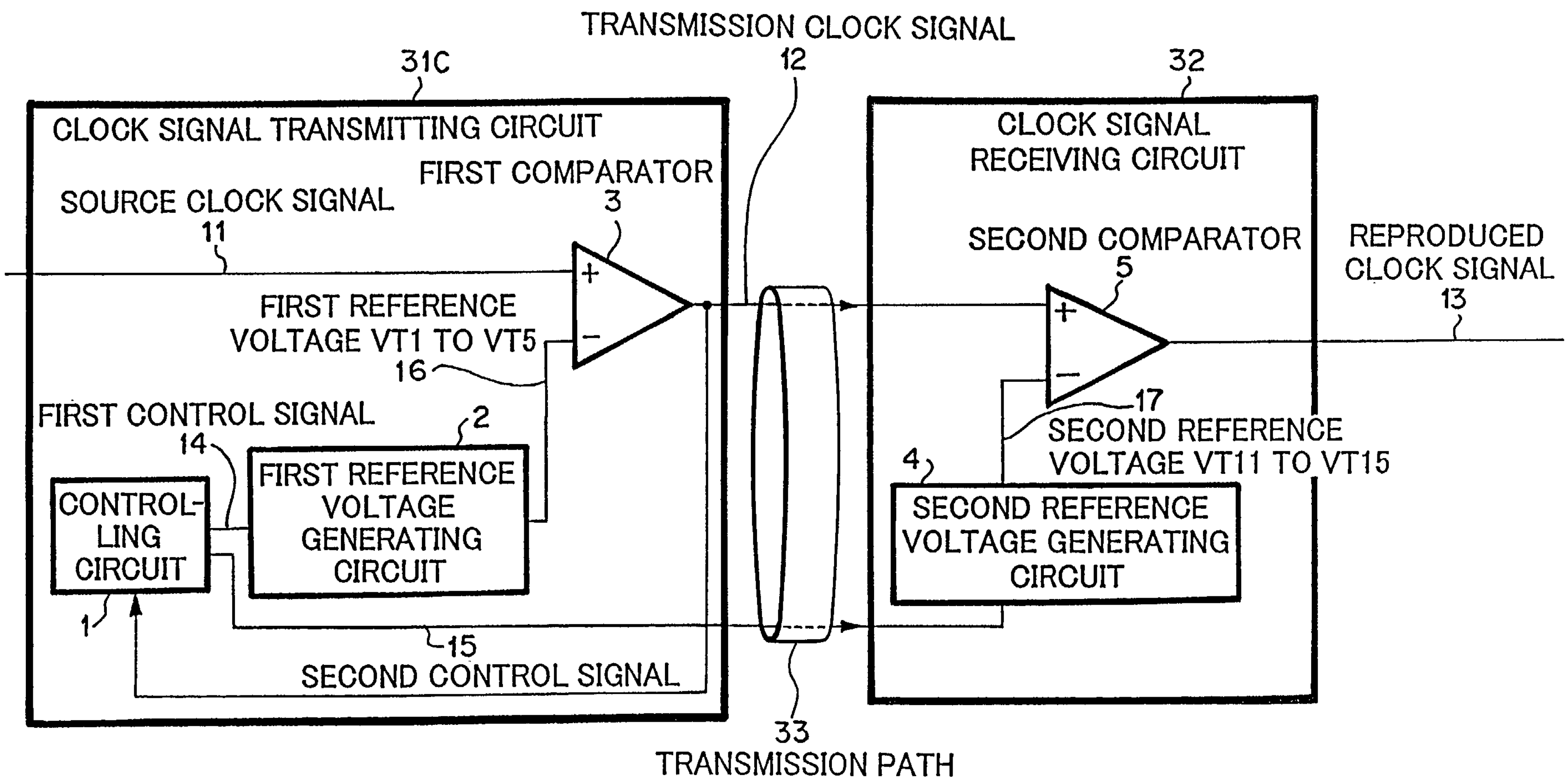


INPUT SIGNAL
VT5 + VH1 / 2
VT1 + VL1 / 2
VH5 + VH1 / 2
CHANGE DETECTION SIGNAL

FIG. 10


START
S601
SET VALUES OF M_c AND N_c
S602
N = 0
S603
M = 0
S604
HAS CHANGE DETECTION SIGNAL BEEN OUTPUT ?
NO
YES
S605
M = M + 1
S606
M = Mc
NO
YES
S607
OUTPUT FIRST CONTROL SIGNAL
S608
N = N + 1
S609
N = Nc
NO
YES
S610
OUTPUT SECOND CONTROL SIGNAL
S611
N = 0

F I G. 11


TRANSMISSION CLOCK SIGNAL
12
31C
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE
VOLTAGE VT1 TO VT5
16
FIRST CONTROL SIGNAL
14
2
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
CONTROLLING CIRCUIT
1
15
SECOND CONTROL SIGNAL
32
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
17
SECOND REFERENCE
VOLTAGE VT11 TO VT15
4
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
33
TRANSMISSION PATH

F I G. 12

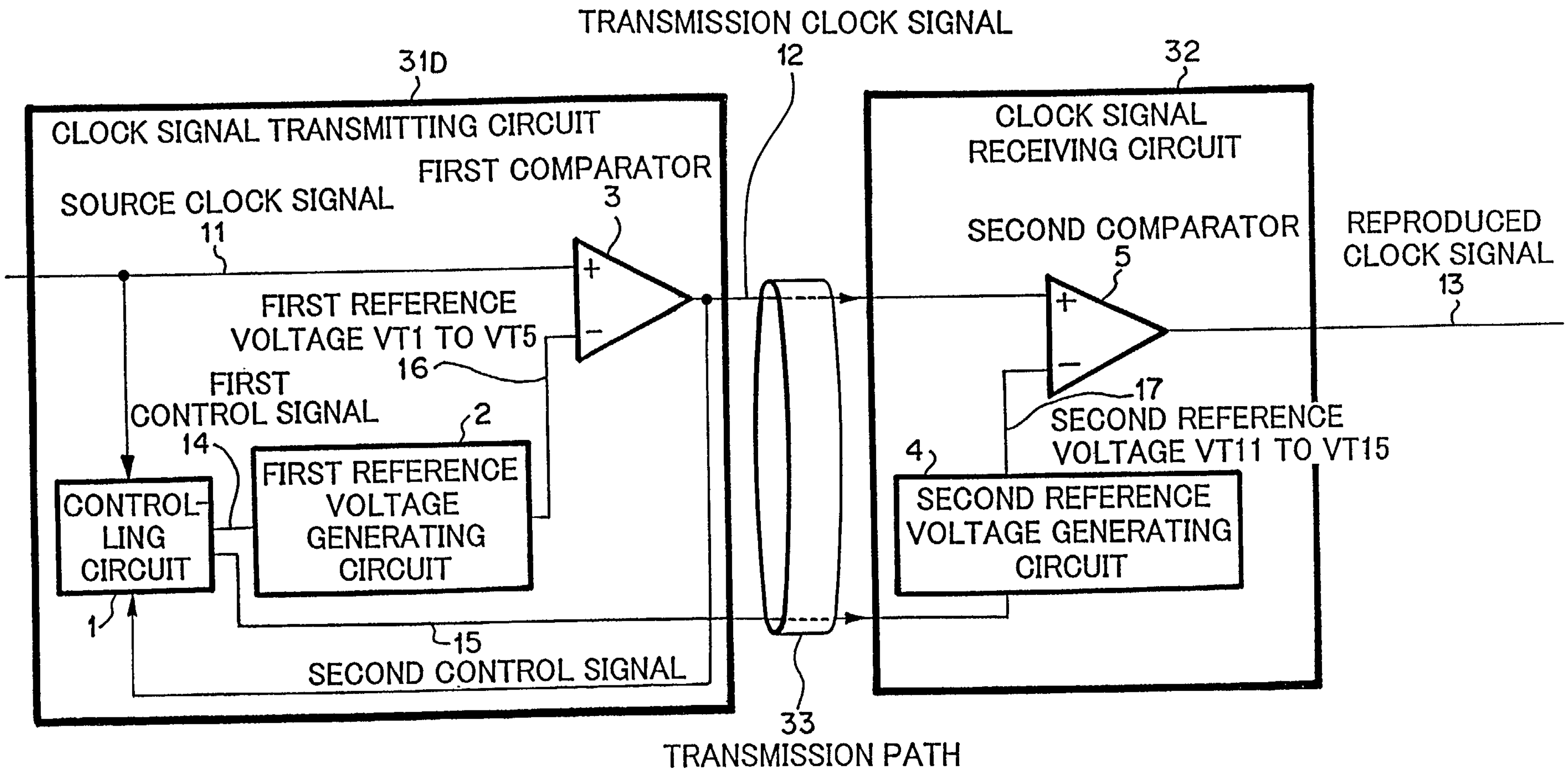

TRANSMISSION CLOCK SIGNAL
12
31D
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE
VOLTAGE VT1 TO VT5
16
FIRST
CONTROL SIGNAL
14
2
FIRST REFERENCE
VOLTAGE
GENERATING
CIRCUIT
CONTROL-
LING
CIRCUIT
1
15
SECOND CONTROL SIGNAL
32
CLOCK SIGNAL
RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED
CLOCK SIGNAL
13
17
SECOND REFERENCE
VOLTAGE VT11 TO VT15
4
SECOND REFERENCE
VOLTAGE GENERATING
CIRCUIT
33
TRANSMISSION PATH

FIG. 13

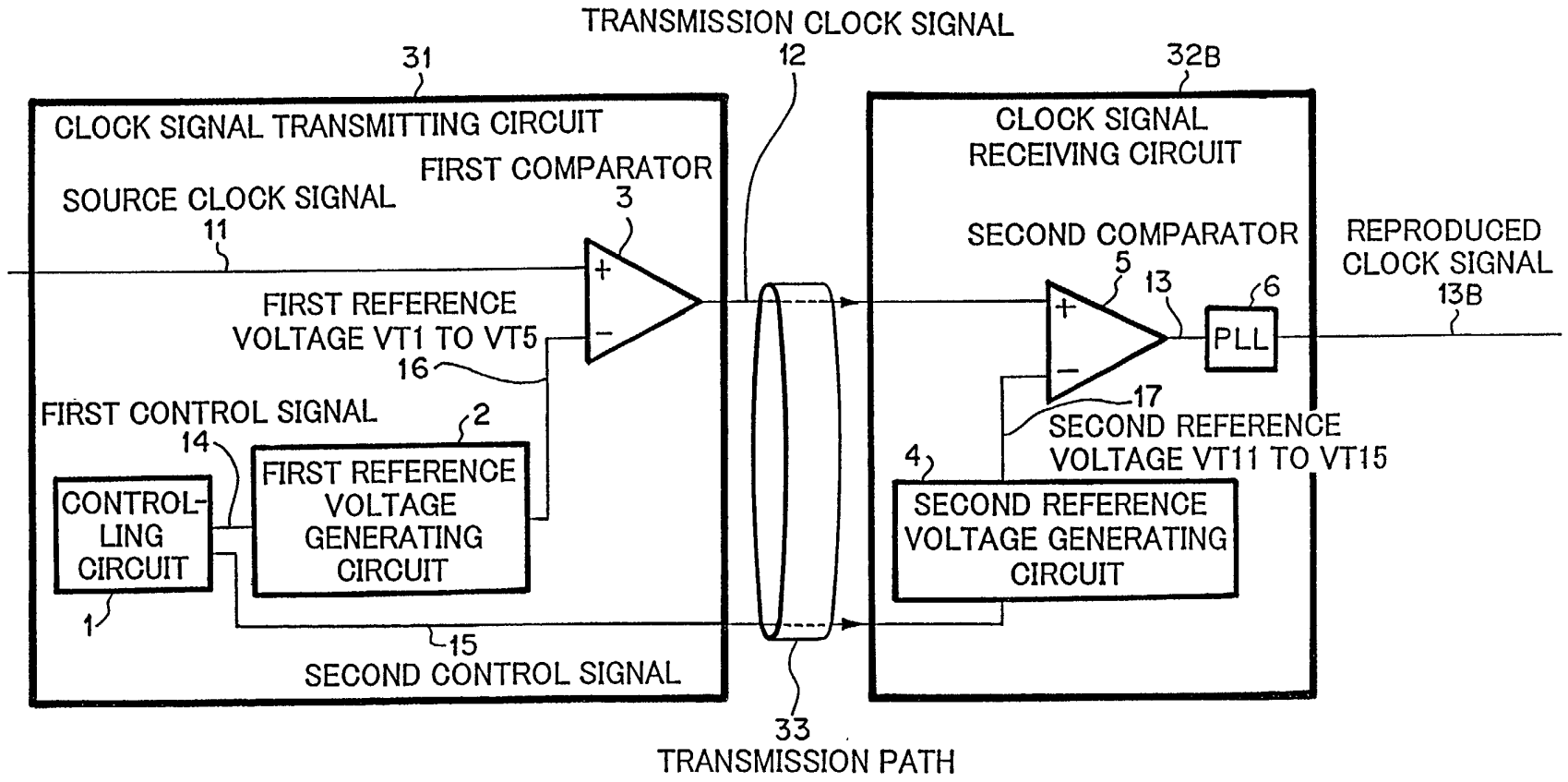

TRANSMISSION CLOCK SIGNAL
31
12
32B
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
13
6
REPRODUCED CLOCK SIGNAL
13B
PLL
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
FIRST CONTROL SIGNAL
14
2
4
CONTROL-LING CIRCUIT
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
1
15
SECOND CONTROL SIGNAL
33
TRANSMISSION PATH

FIG. 14

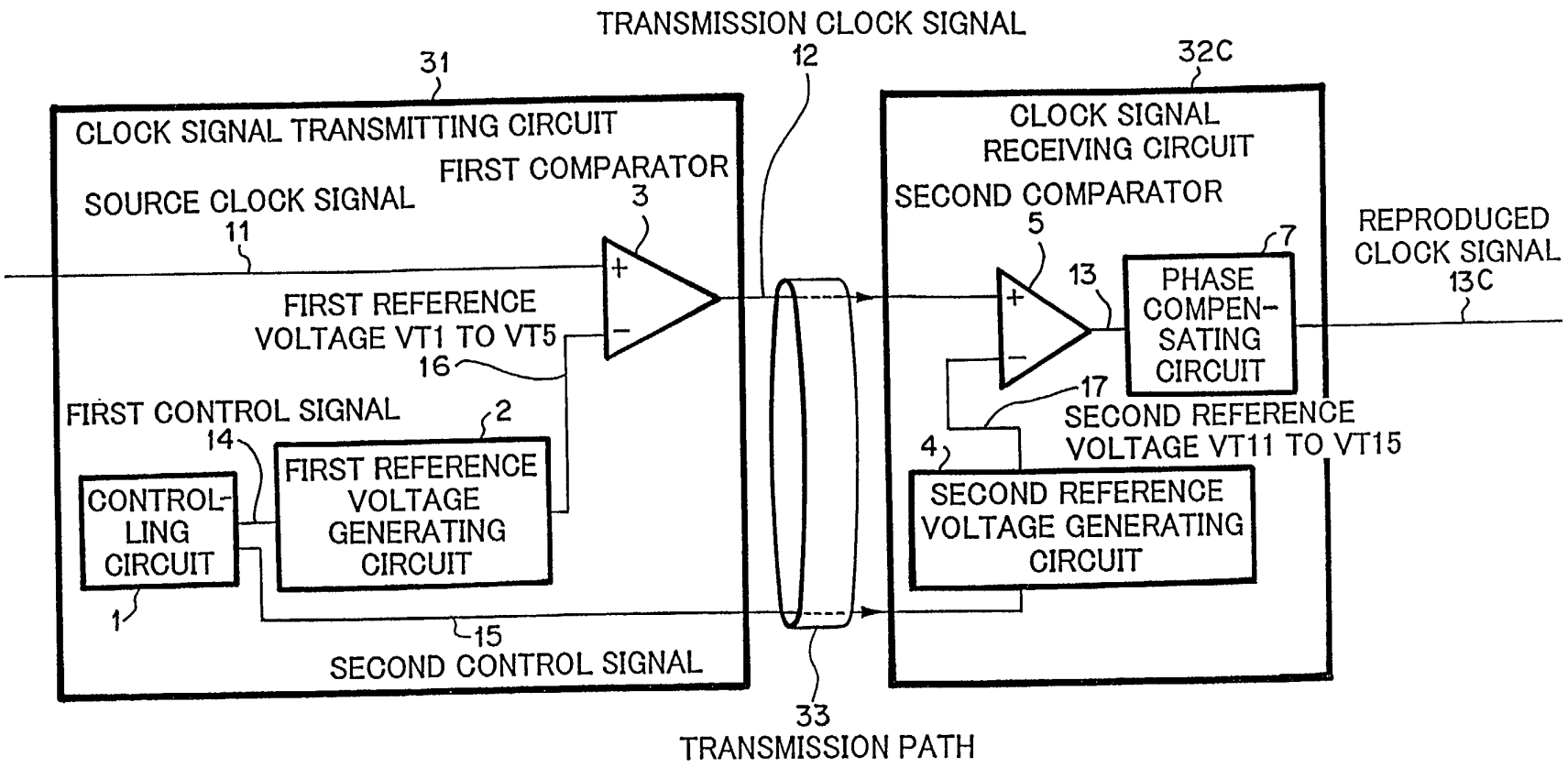
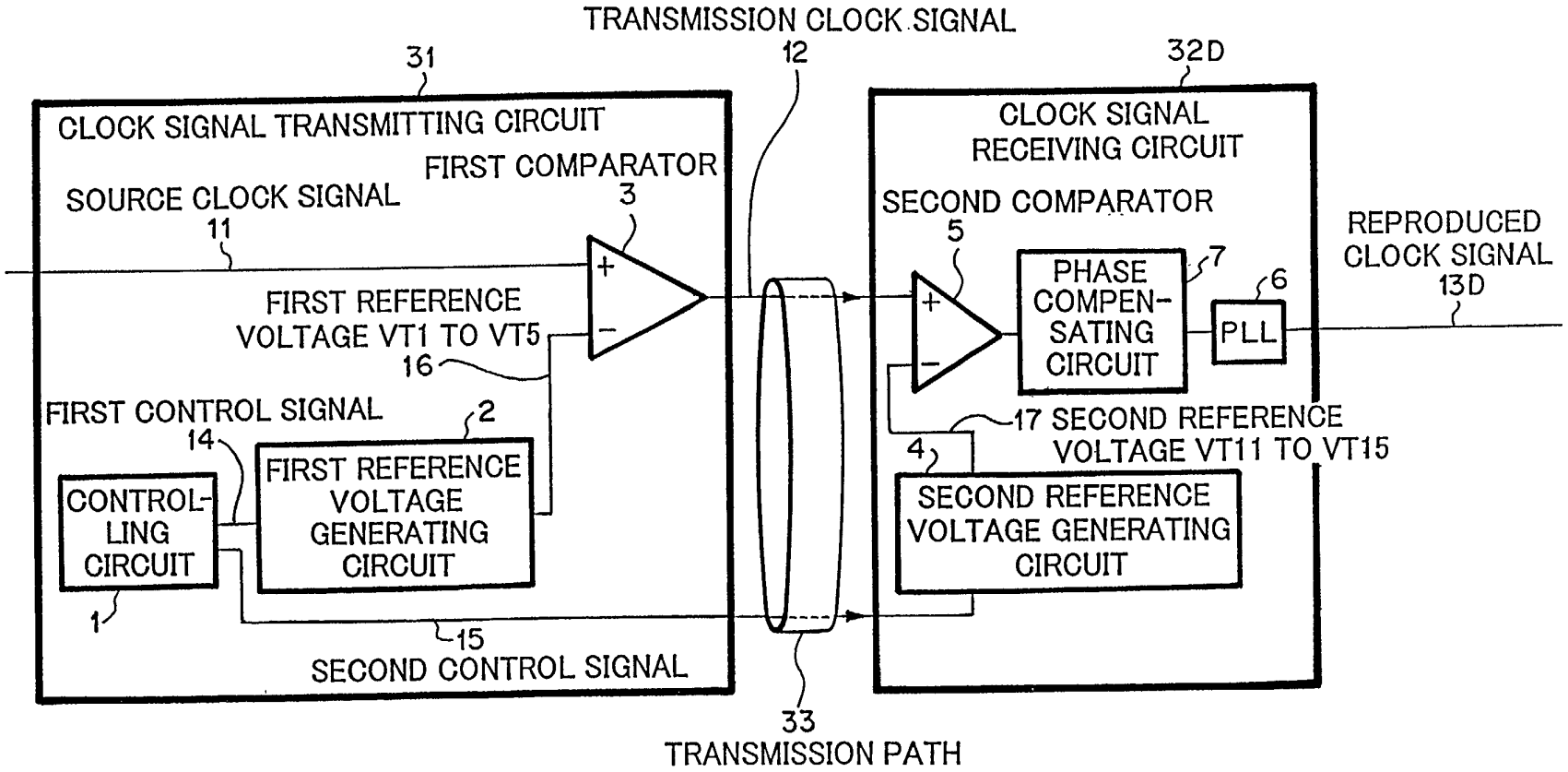
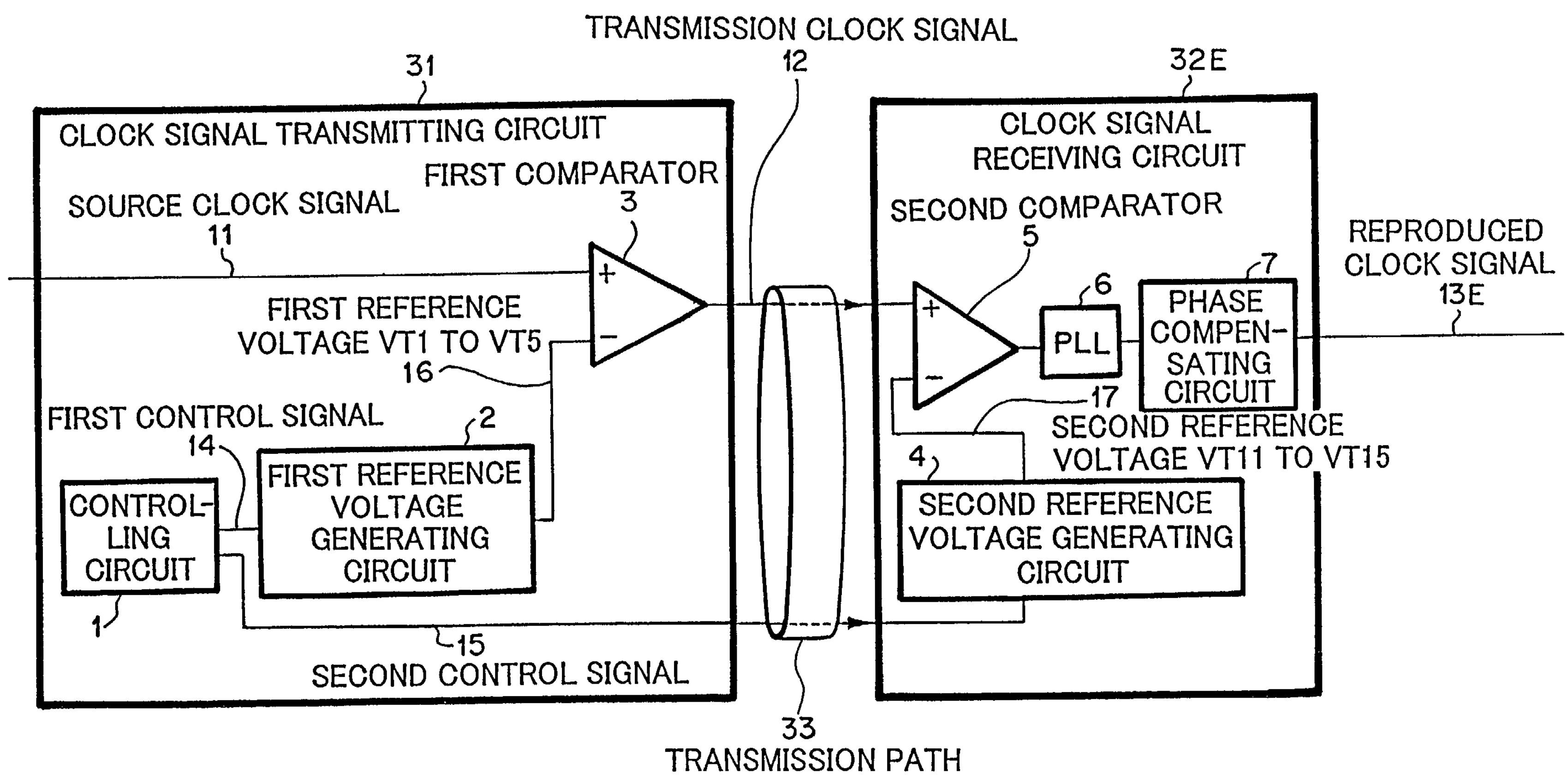


FIG. 15


TRANSMISSION CLOCK SIGNAL
31
12
32D
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13D
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
PHASE COMPEN-SATING CIRCUIT
7
6
PLL
FIRST CONTROL SIGNAL
14
2
17 SECOND REFERENCE VOLTAGE VT11 TO VT15
4
CONTROL-LING CIRCUIT
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
1
15
SECOND CONTROL SIGNAL
33
TRANSMISSION PATH

F I G. 16


TRANSMISSION CLOCK SIGNAL
12
31
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
FIRST CONTROL SIGNAL
14
2
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
CONTROL-LING CIRCUIT
1
15
SECOND CONTROL SIGNAL
32E
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
6
PLL
7
PHASE COMPEN-SATING CIRCUIT
REPRODUCED CLOCK SIGNAL
13E
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
4
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
33
TRANSMISSION PATH

F I G. 17

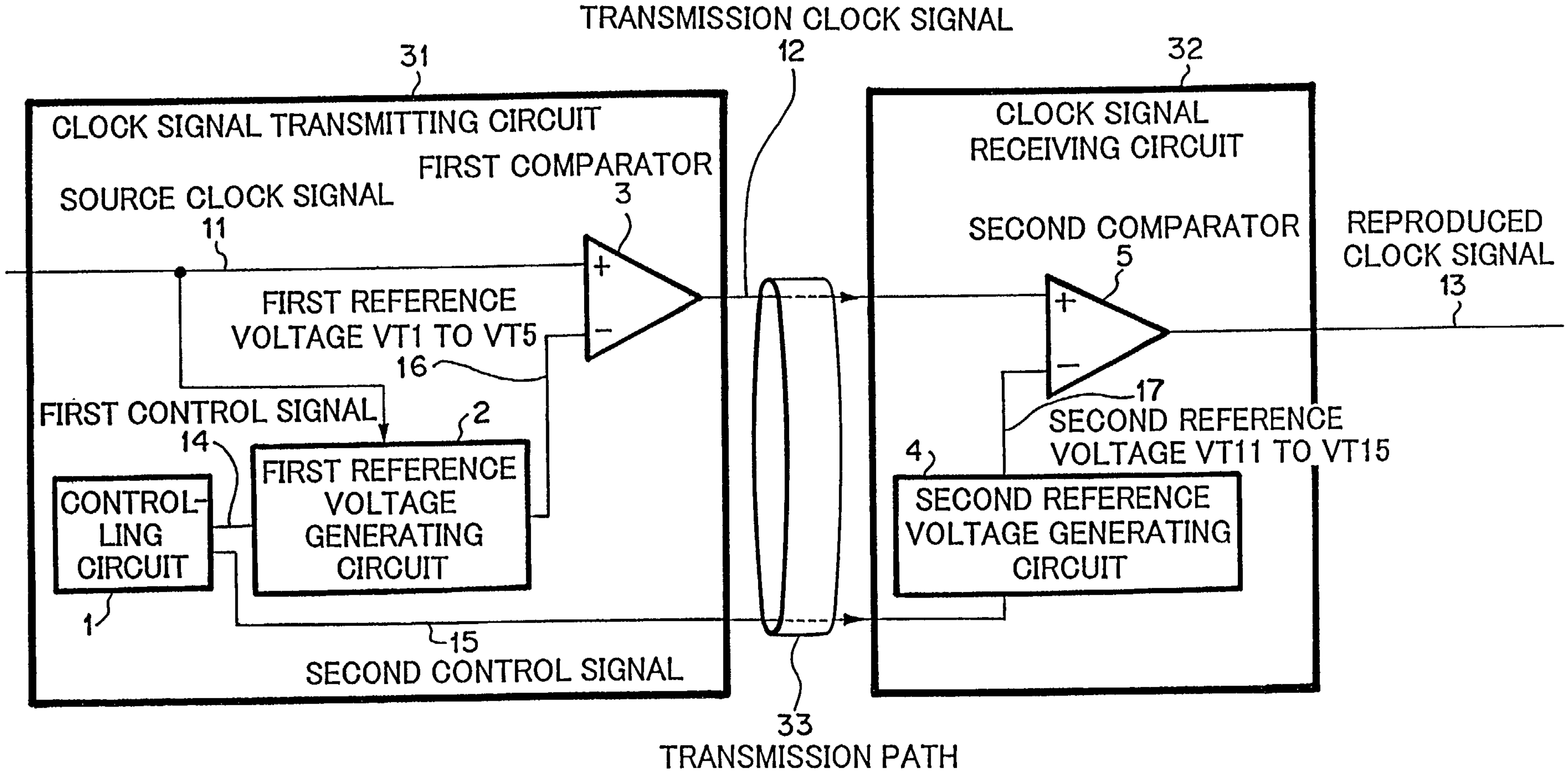

TRANSMISSION CLOCK SIGNAL
12
31
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE
VOLTAGE VT1 TO VT5
16
FIRST CONTROL SIGNAL
14
2
CONTROL-LING CIRCUIT
1
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
15
SECOND CONTROL SIGNAL
32
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
17
SECOND REFERENCE
VOLTAGE VT11 TO VT15
4
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
33
TRANSMISSION PATH

FIG. 18

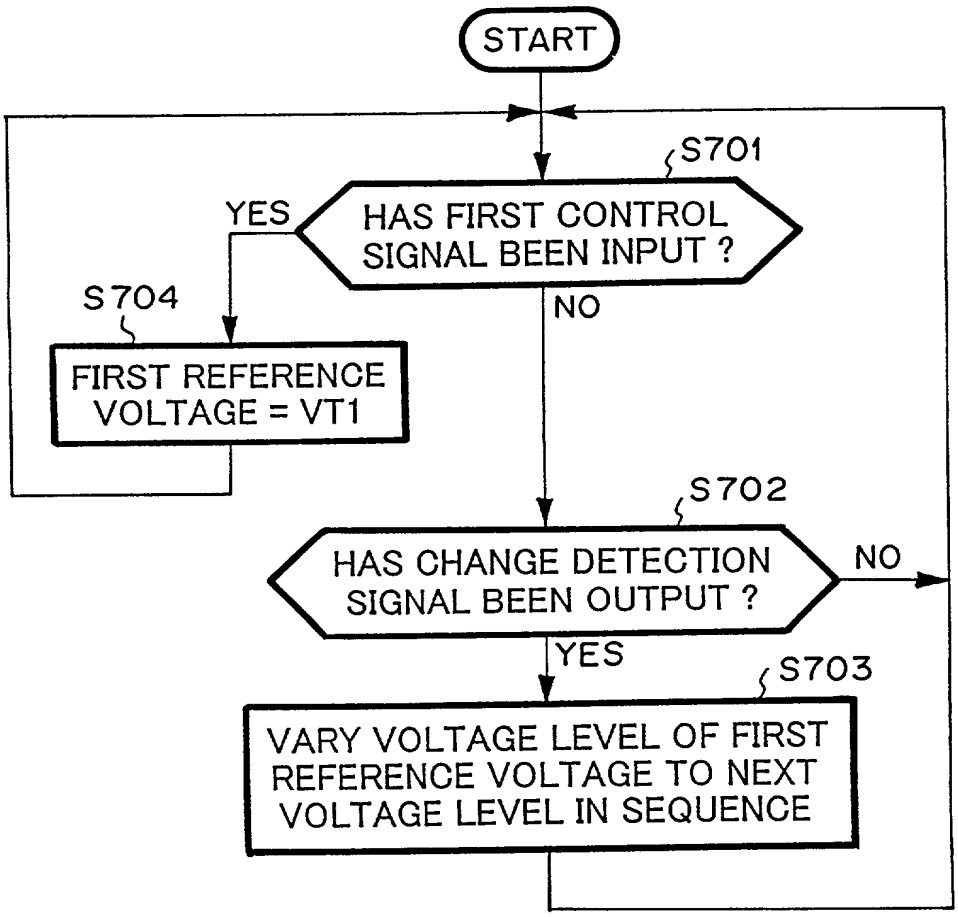

START
S701
HAS FIRST CONTROL SIGNAL BEEN INPUT ?
YES
NO
S704
FIRST REFERENCE VOLTAGE = VT1
S702
HAS CHANGE DETECTION SIGNAL BEEN OUTPUT ?
NO
YES
S703
VARY VOLTAGE LEVEL OF FIRST REFERENCE VOLTAGE TO NEXT VOLTAGE LEVEL IN SEQUENCE

FIG. 19

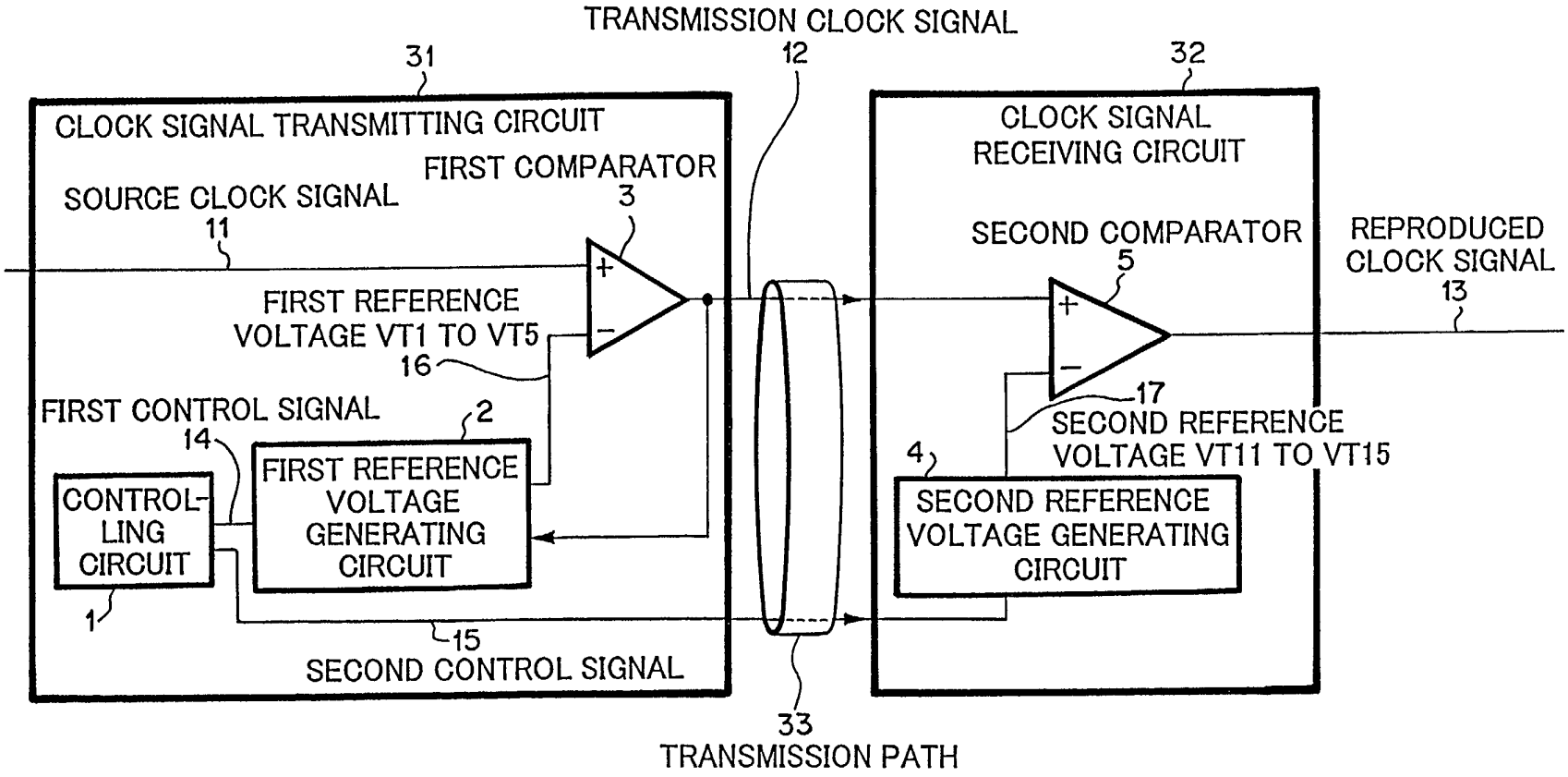
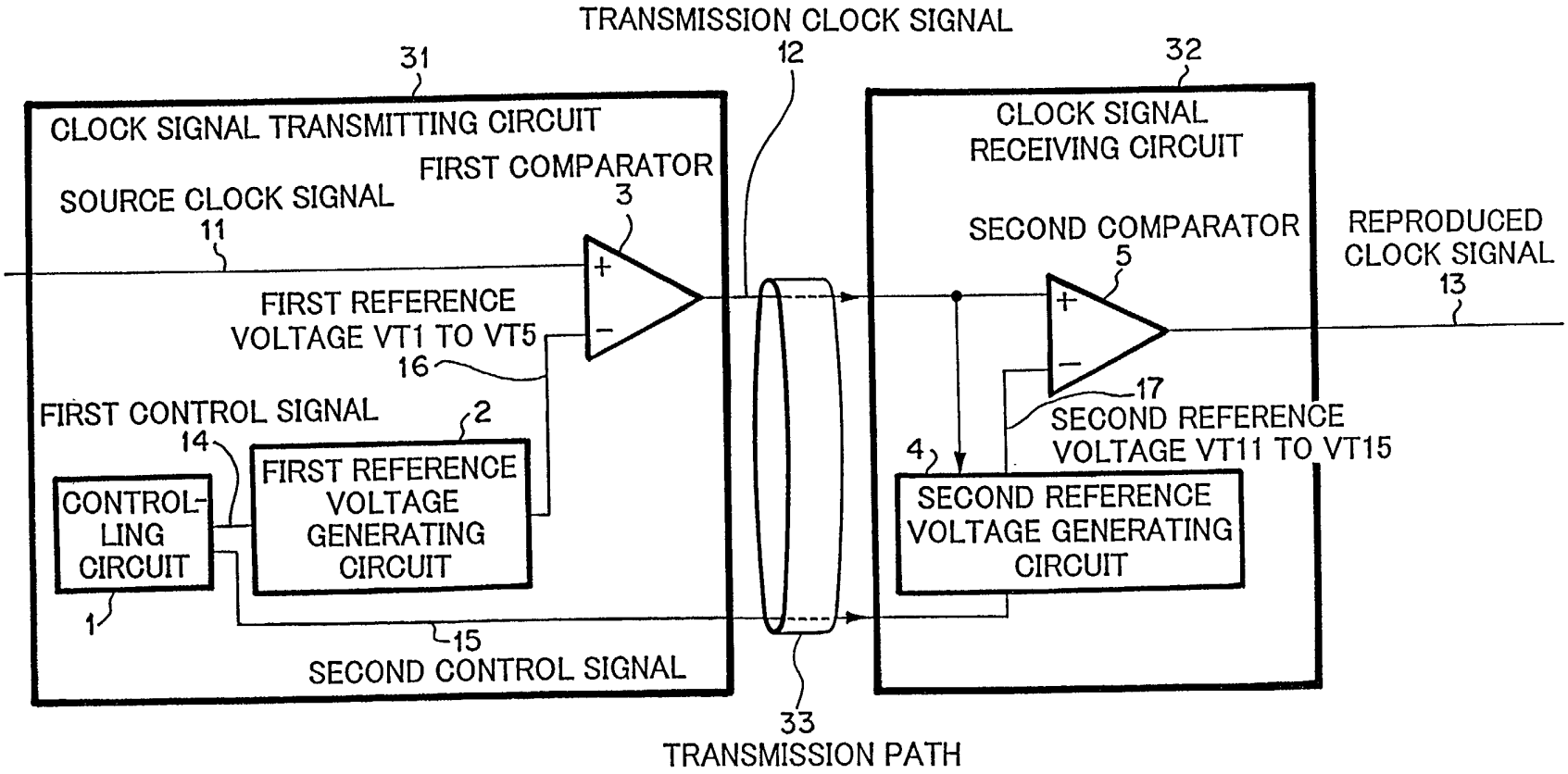
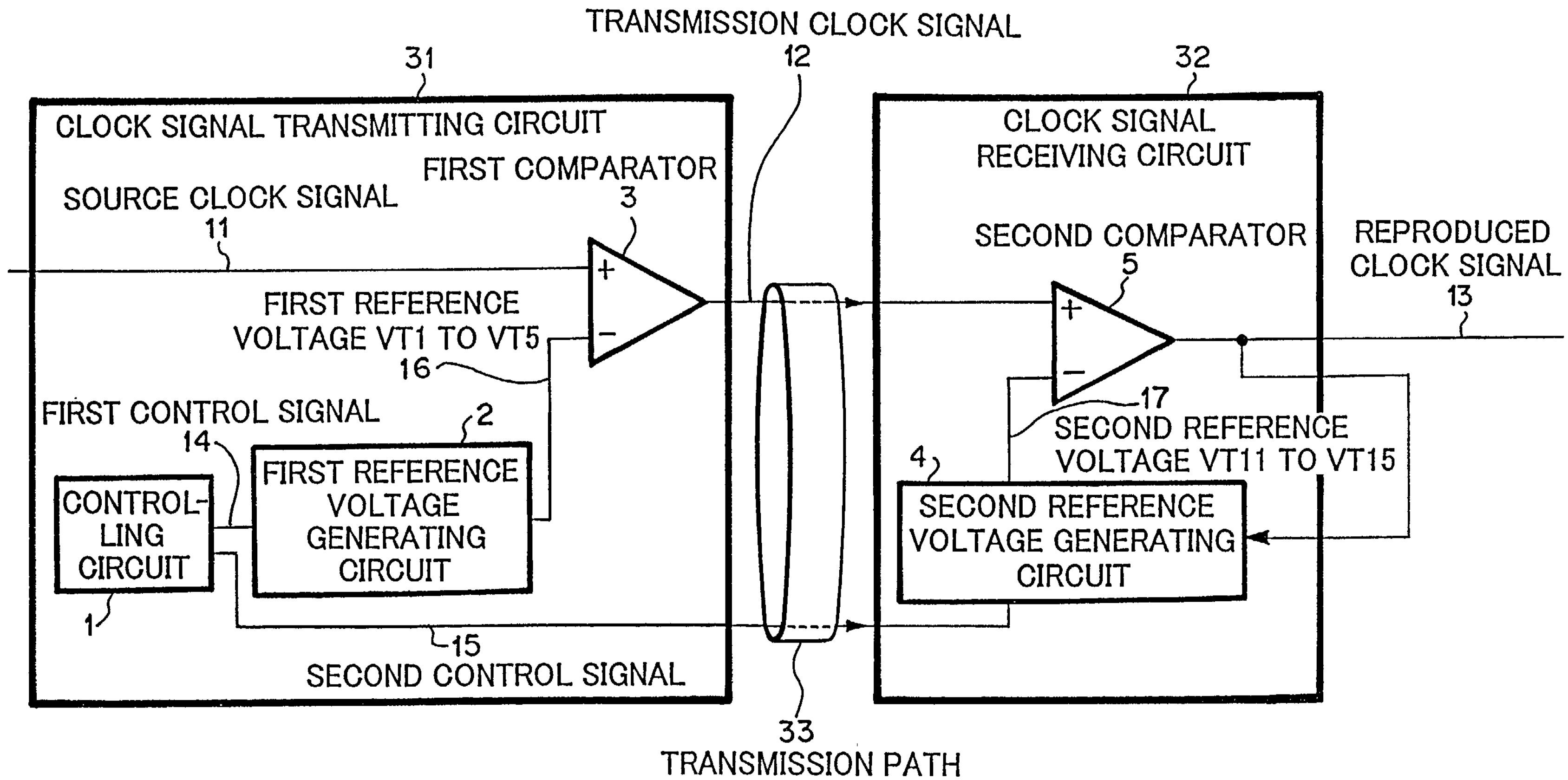


FIG. 20


TRANSMISSION CLOCK SIGNAL
12
31
32
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
FIRST CONTROL SIGNAL
2
14
4
CONTROL-LING CIRCUIT
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
1
15
SECOND CONTROL SIGNAL
33
TRANSMISSION PATH

F I G. 21



TRANSMISSION CLOCK SIGNAL
12
31
CLOCK SIGNAL TRANSMITTING CIRCUIT
SOURCE CLOCK SIGNAL
11
FIRST COMPARATOR
3
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
FIRST CONTROL SIGNAL
14
2
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
CONTROL-LING CIRCUIT
1
15
SECOND CONTROL SIGNAL
32
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
4
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
33
TRANSMISSION PATH

FIG. 22

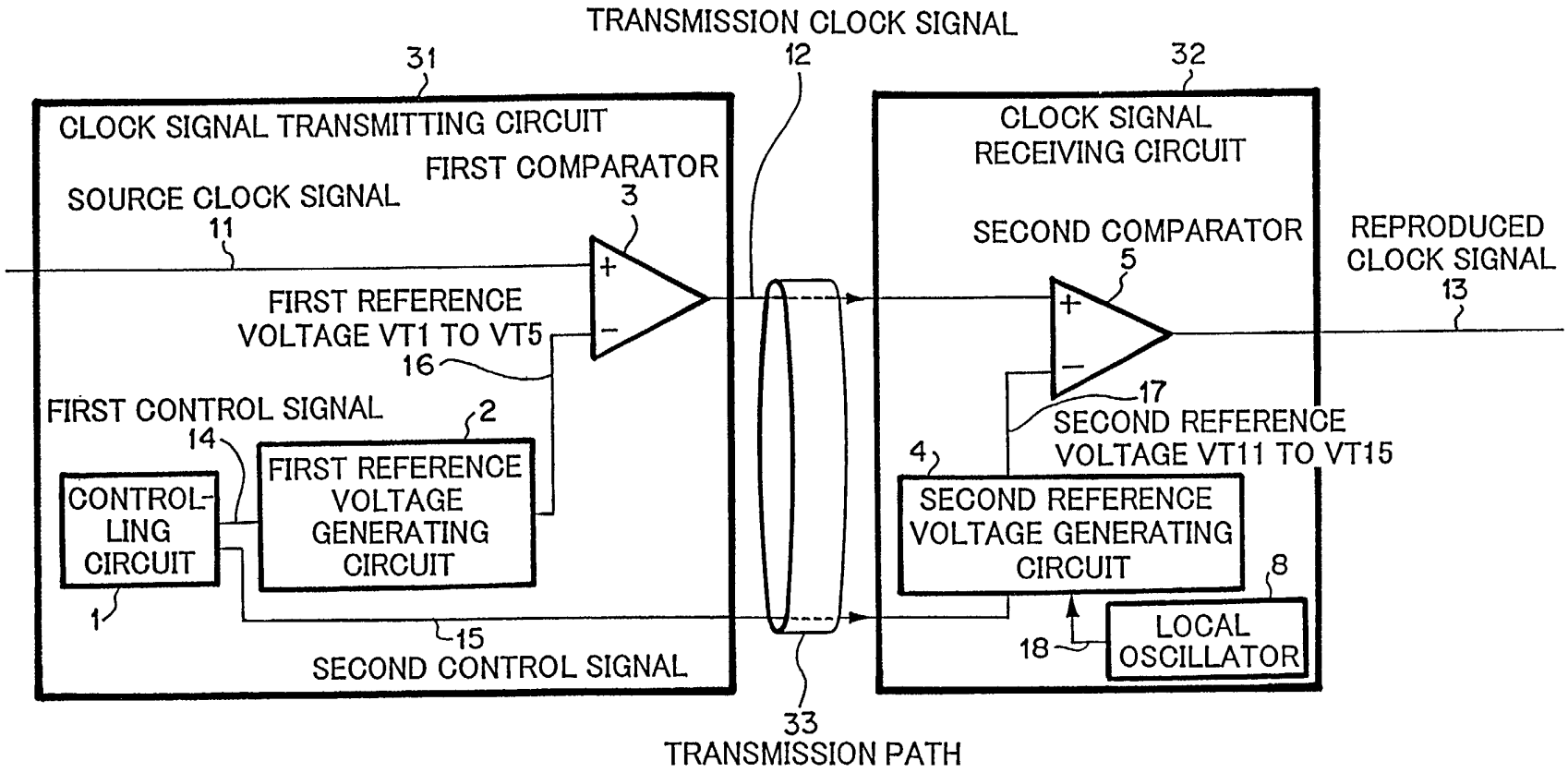
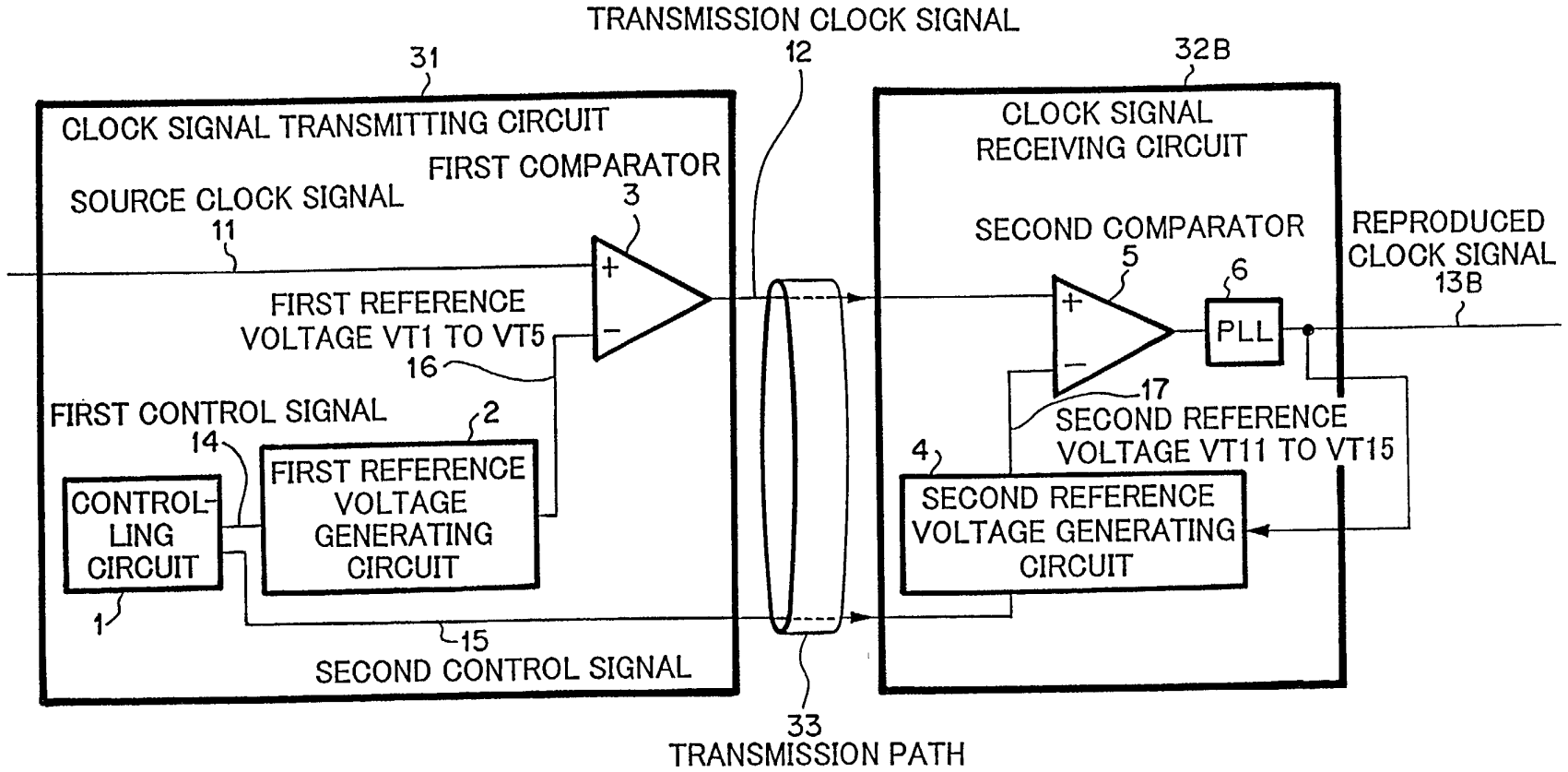
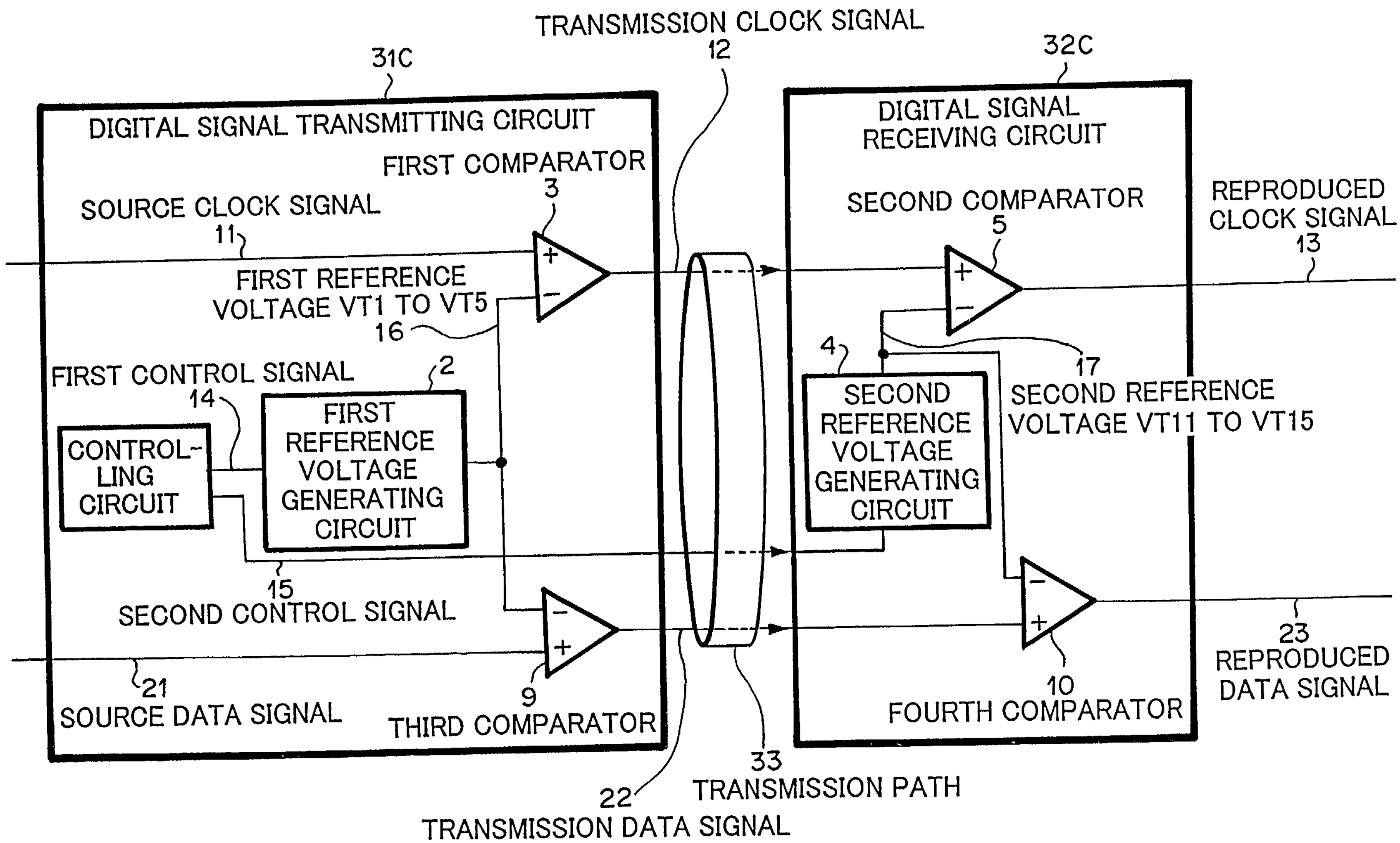

TRANSMISSION CLOCK SIGNAL
31
12
32
CLOCK SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
CLOCK SIGNAL RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED CLOCK SIGNAL
13
FIRST REFERENCE VOLTAGE VT1 TO VT5
16
17
SECOND REFERENCE VOLTAGE VT11 TO VT15
FIRST CONTROL SIGNAL
2
14
4
CONTROL-LING CIRCUIT
FIRST REFERENCE VOLTAGE GENERATING CIRCUIT
SECOND REFERENCE VOLTAGE GENERATING CIRCUIT
8
1
15
18
LOCAL OSCILLATOR
SECOND CONTROL SIGNAL
33
TRANSMISSION PATH

FIG.23

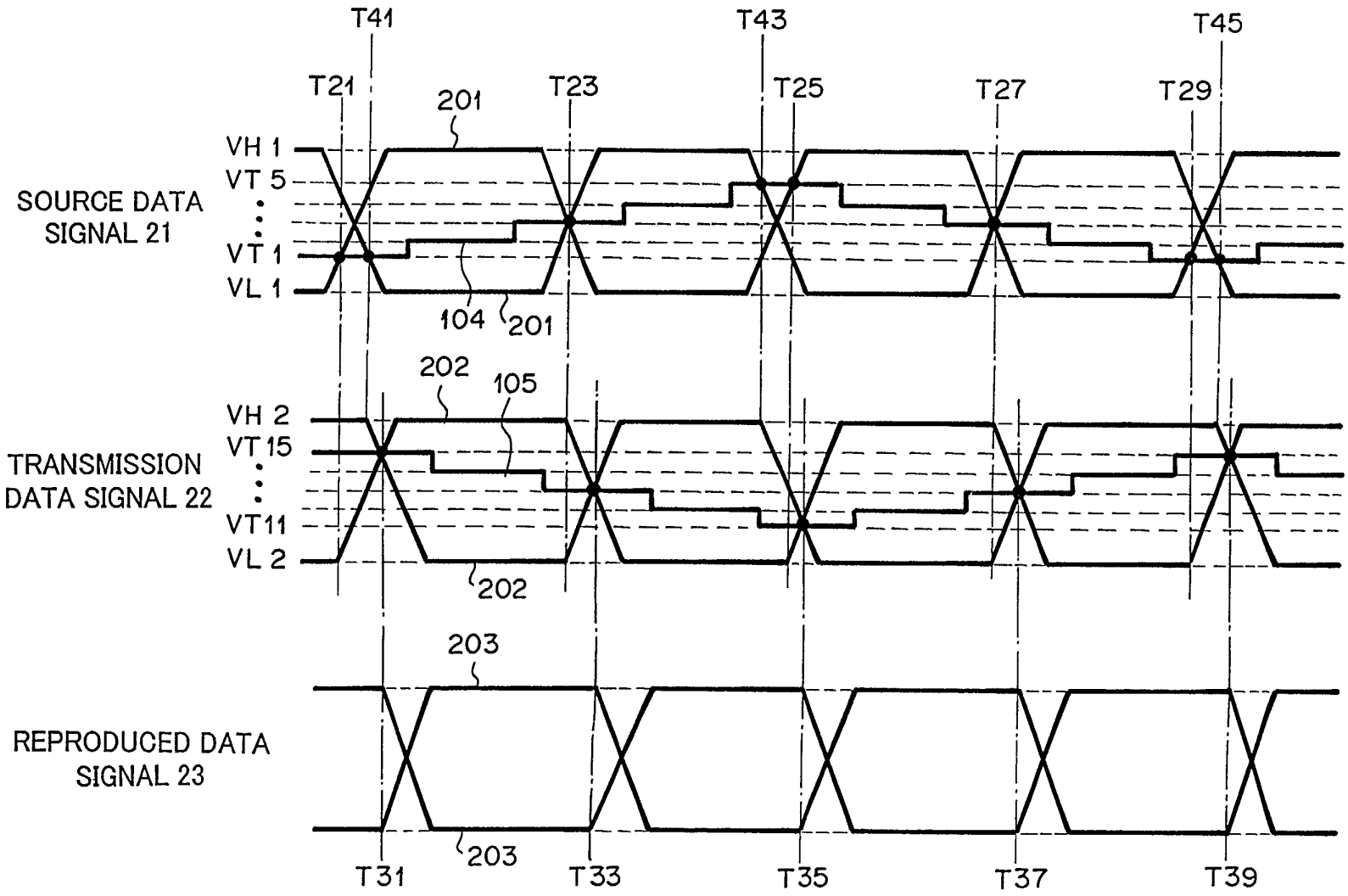


F I G . 24



TRANSMISSION CLOCK SIGNAL
12
31C
DIGITAL SIGNAL TRANSMITTING CIRCUIT
FIRST COMPARATOR
3
SOURCE CLOCK SIGNAL
11
FIRST REFERENCE
VOLTAGE VT1 TO VT5
16
FIRST CONTROL SIGNAL
14
2
CONTROL-
LING
CIRCUIT
FIRST
REFERENCE
VOLTAGE
GENERATING
CIRCUIT
15
SECOND CONTROL SIGNAL
21
SOURCE DATA SIGNAL
9
THIRD COMPARATOR
32C
DIGITAL SIGNAL
RECEIVING CIRCUIT
SECOND COMPARATOR
5
REPRODUCED
CLOCK SIGNAL
13
4
SECOND
REFERENCE
VOLTAGE
GENERATING
CIRCUIT
17
SECOND REFERENCE
VOLTAGE VT11 TO VT15
10
FOURTH COMPARATOR
23
REPRODUCED
DATA SIGNAL
33
TRANSMISSION PATH
22
TRANSMISSION DATA SIGNAL

FIG. 25



F-10600

Declaration and Power of Attorney for Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明として、以下の通り宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CLOCK SIGNAL TRANSMITTING SYSTEM,
DIGITAL SIGNAL TRANSMITTING SYSTEM,
CLOCK SIGNAL TRANSMITTING METHOD,
AND DIGITAL SIGNAL TRANSMITTING METHOD

その明細書を
（該当するほうに印を付す）

the specification of which
(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ _____ 日に出願番号 第 _____ 号として提出し、

☐ was filed on _____ as Application Serial No. _____

_____ 日に補正した。
（該当する場合）

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第1章第56条(a)項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119条、第172条、又は第365条に基づく下記の外国特許出願又は発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願又は発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

			Priority claimed 優先権の主張	
327198/1999 (Number) (番号)	Japan (Country) (国名)	17/11/1999 (Day/Month/Year Filed) (出願の年月日)	☒ Yes あり	☐ No なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)	☐ Yes あり	☐ No なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)	☐ Yes あり	☐ No なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)	☐ Yes あり	☐ No なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)	☐ Yes あり	☐ No なし

私は、合衆国法典第35部第120条に基づく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日又はＰＣＴ国際出願日の間に公表された連邦規則法典第37部第1章第56条(a)項に記載の所要の情報を開示すべき義務を有することを認める。

I hereby claim the benefit of Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose any material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現況) 特許済み、係属中、放棄済み	(Status) (patended, pending abandoned)
(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現況) 特許済み、係属中、放棄済み	(Status) (patended, pending abandoned)

私は、ここに自己の知識に基づいて行った陳述がすべて真実であり、自己の有する情報及び信ずるところに従って行った陳述が真実であると信じ、更に故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁固に処せられるか、又はこれらの刑が併科され、又はかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true; and further that all statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Japanese Language Declaration

委任状： 私は、下記発明者として、以下の代理人をここに選任し、本願の手続きを遂行すること並びにこれに関する一切の行為を特許商標局に対して行うことを委任する。
（代理人氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg. No. 32,765, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

書類の送付先： Send Correspondence to:

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037

直通電話連絡先： （名称及び電話番号） Direct Telephone Calls to: *(name and telephone number)*

(202)293-7060

唯一の又は第一の発明者の氏名	Full name of sole or first inventor Masahiro ARAI
同発明者の署名 日付	Inventor's signature Date Masahiro Arai November 6, 2000
住所	Residence Tokyo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post office address c/o NEC Corporation, 7-1,
	Shiba 5-chome, Minato-ku, Tokyo, Japan
第二の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any
同第二発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post office address

（第三又はそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)